TAN-065
Application Note

Physical Interface

XRT86VL3x DS-1/E1 Framer + LIU Combo

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1.0 GENERAL DESCRIPTION AND INTERFACE

The XRT86VL3x supports multiple interfaces for various modes of operation. The purpose of this section is to present a general overview of the common interfaces and their connection diagrams. Each mode will be described in full detail in later sections of the datasheet.

NOTE: *For a brief tutorial on Framing Formats, see Appendix A in the back of this document.*

1.1 Physical Interface

The Line Interface Unit generates/receives standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68µF and a 1:2 step-up transformer. The receive path inputs only require one bypass capacitor of 0.1µF connected to the center tap (CT) of the transformer and a 1:1 transformer. The receive CT bypass capacitor is required for Long Haul Applications, and recommended for Short Haul Applications. **Figure 1** shows the typical connection diagram for the LIU transmitters. **Figure 2** shows a typical connection diagram for the LIU receivers.

FIGURE 1. LIU TRANSMIT CONNECTION DIAGRAM USING INTERNAL TERMINATION

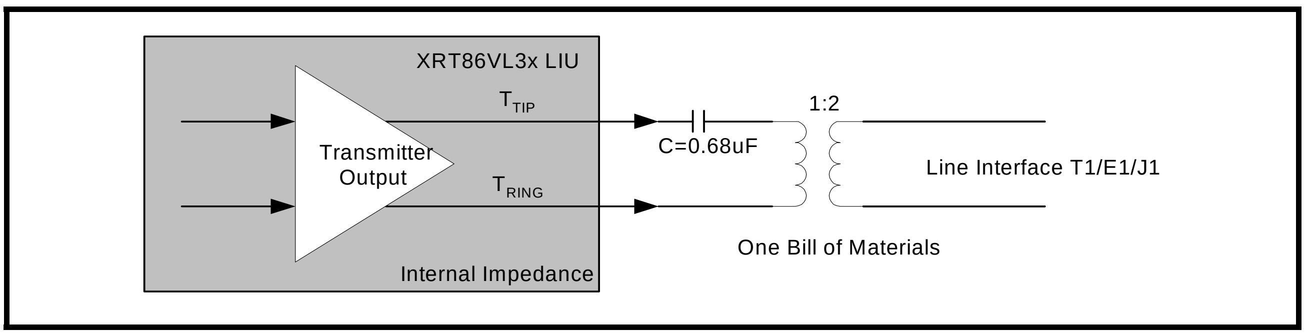
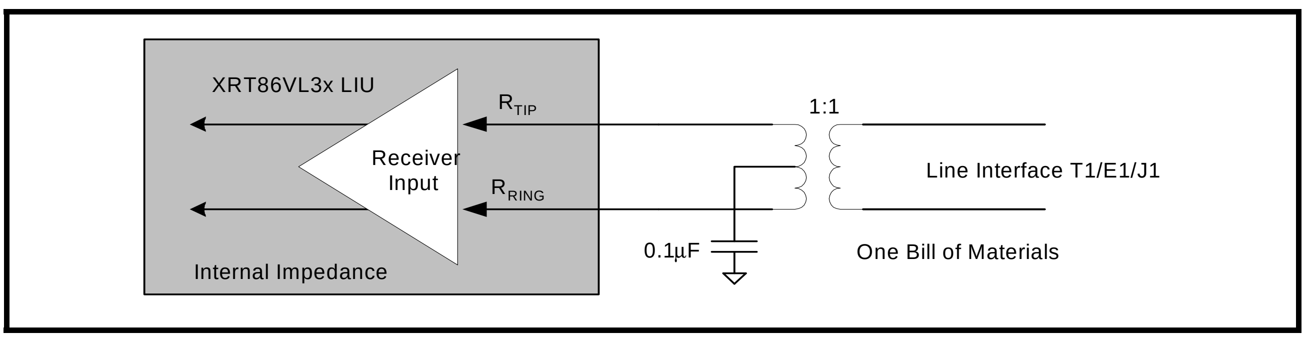


FIGURE 2. LIU RECEIVE CONNECTION DIAGRAM USING INTERNAL TERMINATION



1.2 RT1/E1 Serial PCM Interface

The most common mode is the standard serial PCM interface. Within this mode, only the serial data, serial clock, frame pulse and multi-frame pulse are required for both the transmit and receive paths. For the transmit path, only TxSER is a dedicated input to the device. All other signals to the transmit path in **Figure 3** can be programmed as either input or output. For the receive path, only RxSER and RxMSYNC are dedicated outputs from the device. All other signals in the receive path in **Figure 4** can be programmed as either input or output.

FIGURE 3. TRANSMIT T1/E1 SERIAL PCM INTERFACE

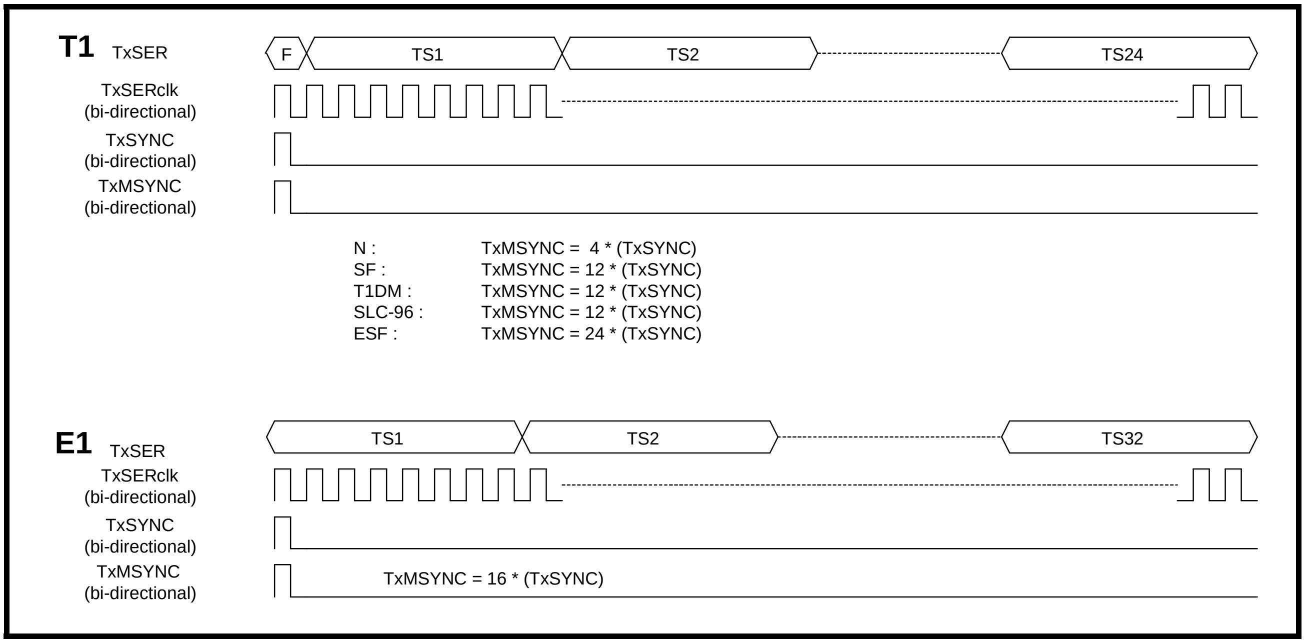
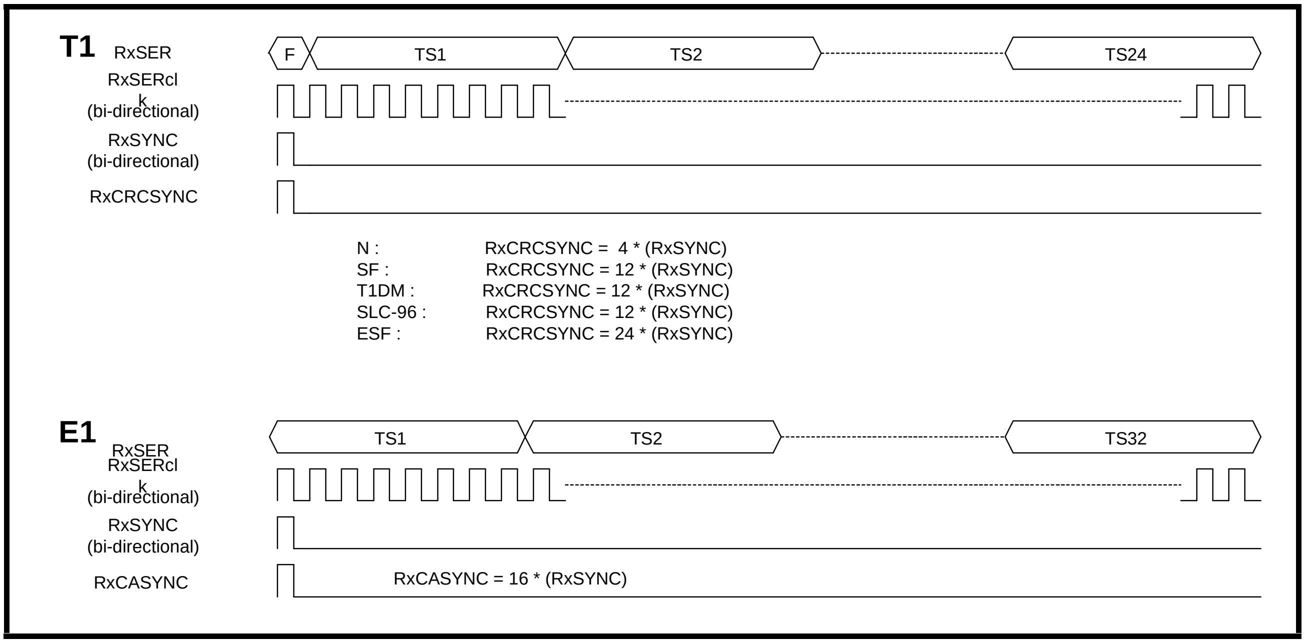


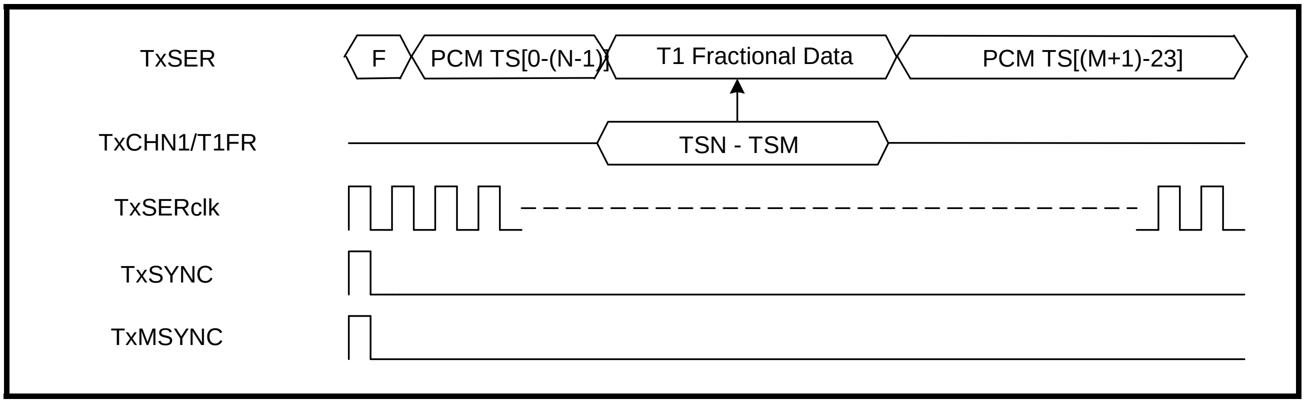
FIGURE 4. RECEIVE T1/E1 SERIAL PCM INTERFACE



1.3 T1/E1 Fractional Interface

The individual time slots can be enabled/disabled to carry fractional DS-0 data. The purpose of this interface is to enable one or more time slots in the PCM data (TxSER) to be replaced with the fractional DS-0 payload. If this mode is selected, the dedicated hardware pin TxCHN1/T1FR is used to input the fractional DS-0 data within the time slots that are enabled. The dedicated hardware pin RxCHN1/R1FR is used to output the fractional DS-0 data within the time slots that are enabled. **Figure 5** is a simplified diagram of the Fractional Interface.

FIGURE 5. T1 FRACTIONAL INTERFACE

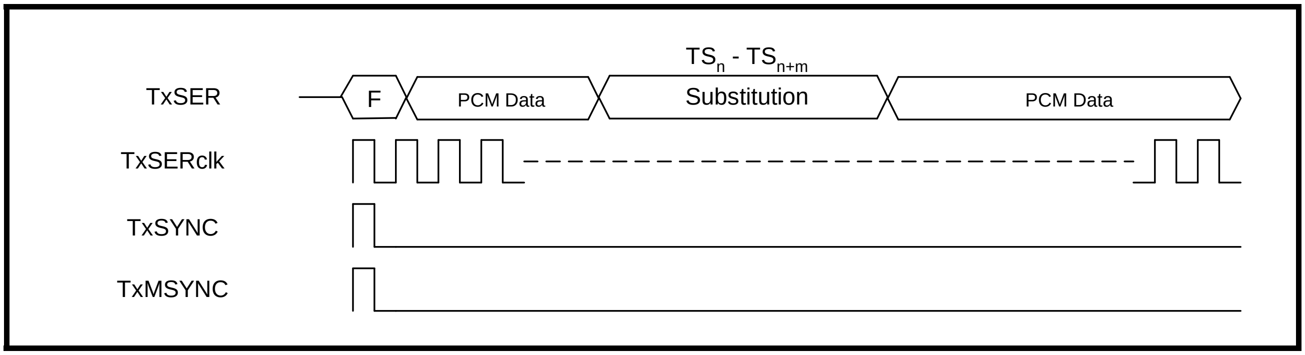


1.4 T1/E1 Time Slot Substitution and Control

The time slots within PCM data are reserved for carrying individual DS-0's. However, the framer block (transmit or receive paths) can substitute the payload with various code definitions. Each time slot can be independently programmed to carry normal PCM data or a variety of user codes. In E1 mode, the user can substitute the transmit time slots 0 and 16, although signaling and Frame Sync cannot be maintained. The following options for time slot substitution are available:

- Unchanged
- Invert all bits
- Invert even bits
- Invert odd bits
- Programmable User Code
- Busy 0xFF
- Vacant 0xD5
- Busy TS, Busy 00
- A-Law, µ-Law
- Invert the MSB bit
- Invert all bits except the MSB bit
- PRBS
- D/E Channel (or Fractional Input)

FIGURE 6. T1/E1 TIME SLOT SUBSTITUTION AND CONTROL



1.5 Robbed Bit Signaling/CAS Signaling

Signaling is used to convey status information relative to the individual DS-0's. If a particular DS-0 is On Hook, Off Hook, etc. this information is carried within the robbed bits in T1 (SF/ESF/SLC-96) or the sixteenth time slot in E1. On the transmit path, the Signaling information can be inserted through the PCM data, internal registers, or a dedicated external Signaling Bus by programming the appropriate registers. On the receive path, the signaling information is extracted (if enabled) to the internal registers and the external signaling bus in addition to being embedded within the PCM data. If the user wishes to substitute the ABCD values, the substitution only occurs in the PCM data. Once substituted, the internal registers and the external signaling bus will not be affected. Figure 7 is a simplified block diagram showing the Signaling Interface. Figure 8 is a timing diagram showing how to insert the ABCD values for each time slot in ESF / CAS. Figure 9 is a timing diagram showing how to insert the AB values for SF / SLC-96 or 4-code signaling in ESF / CAS.

FIGURE 7. ROBBED BIT SIGNALING / CAS SIGNALING

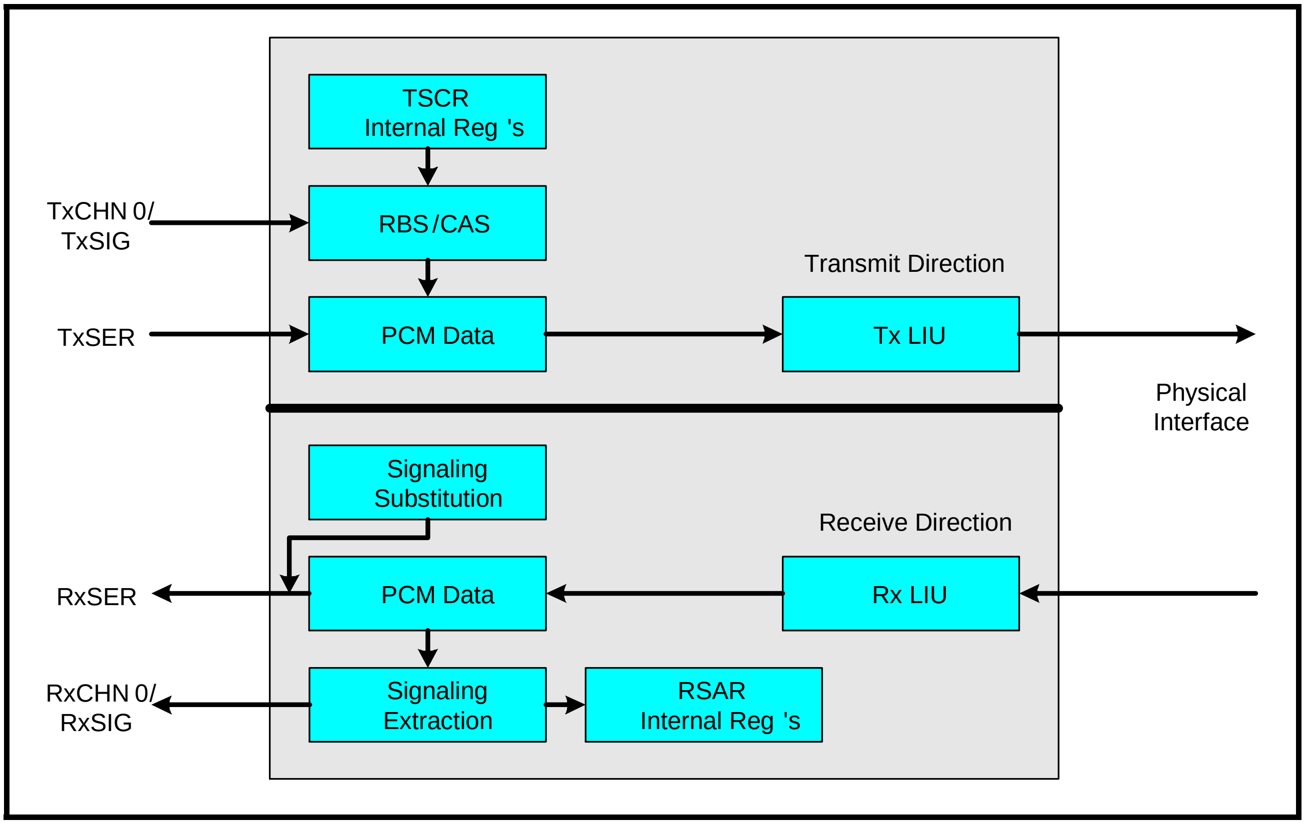


FIGURE 8. ESF / CAS EXTERNAL SIGNALING BUS

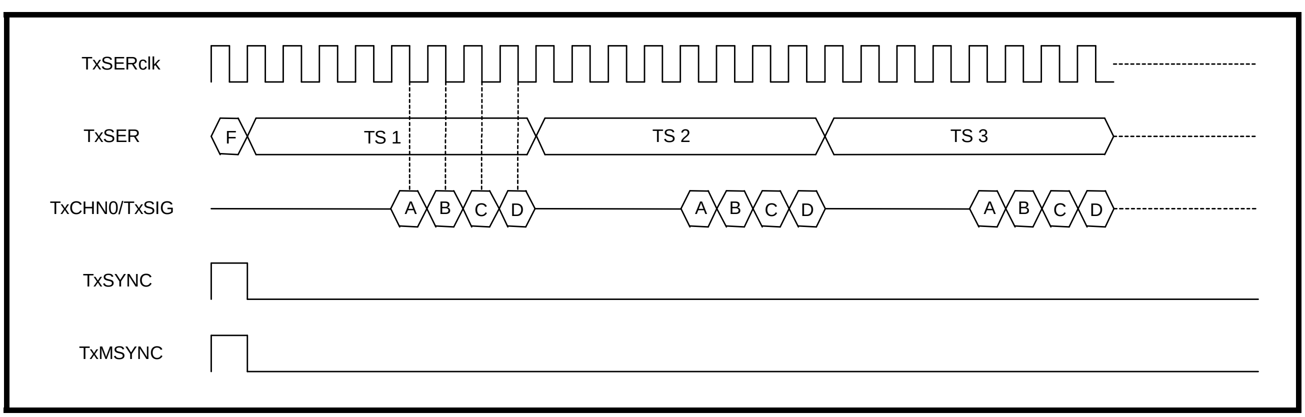
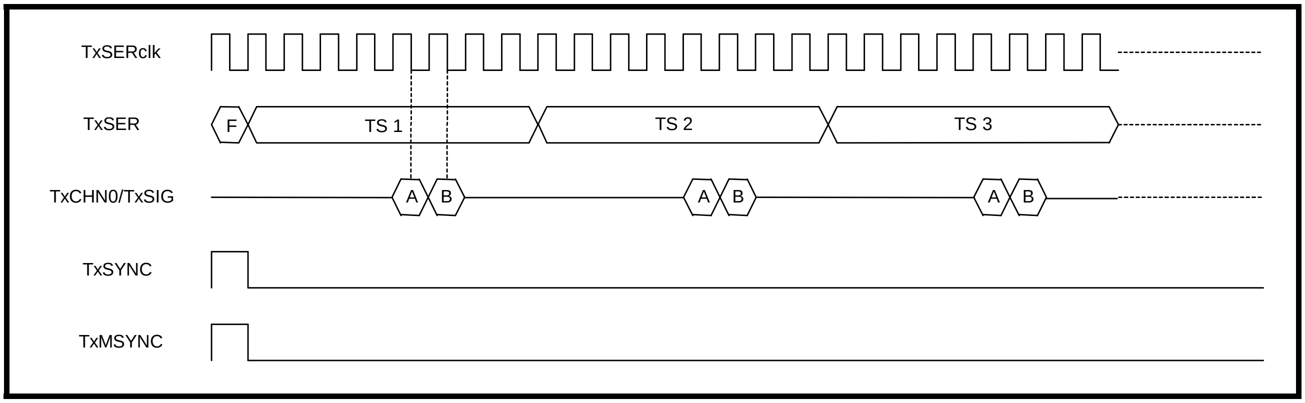


FIGURE 9. SF / SLC-96 OR 4-CODE SIGNALING IN ESF / CAS EXTERNAL SIGNALING BUS



1.6 Overhead Interface

The Overhead interface provides an option for inserting the datalink bits into the transmit PCM data or extracting the datalink bits from the receive PCM data. By default, the datalink information is processed to and from the PCM data directly. On the transmit path, the overhead clock is automatically provided as a clock reference to externally time the datalink bits. The user should provide data on the rising edge of the TxOHclk so that the framer can sample the datalink bits on the falling edge. On the receive path, the datalink bits are updated on the rising edge of the RxOHclk output pin. In T1 ESF mode, a datalink bit occurs every other frame. Therefore, the default overhead interface is operating at 4kbps. In E1 mode, the datalink bits are located in the first time slot of each Non-FAS frame. Figure 10 is a simplified block diagram of the Overhead Interface. Figure 11 is a simplified diagram for the T1 external overhead datalink bus. Figure 12 is a simplified diagram for the E1 external overhead datalink bus.

FIGURE 10. T1/E1 OVERHEAD INTERFACE

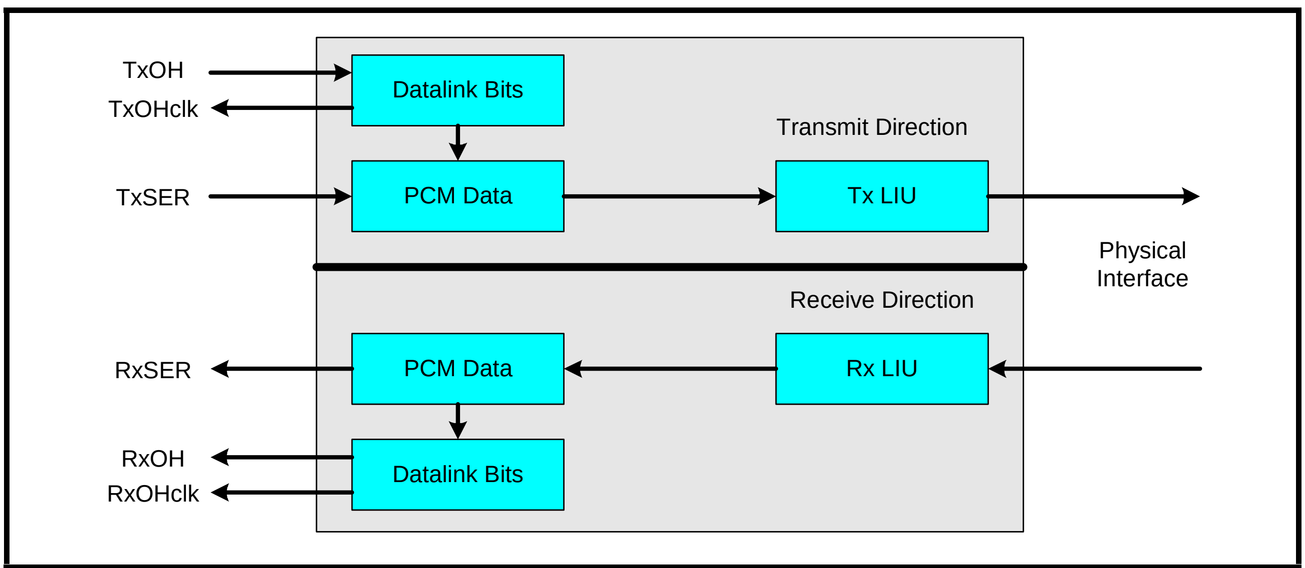


FIGURE 11. T1 EXTERNAL OVERHEAD DATALINK BUS

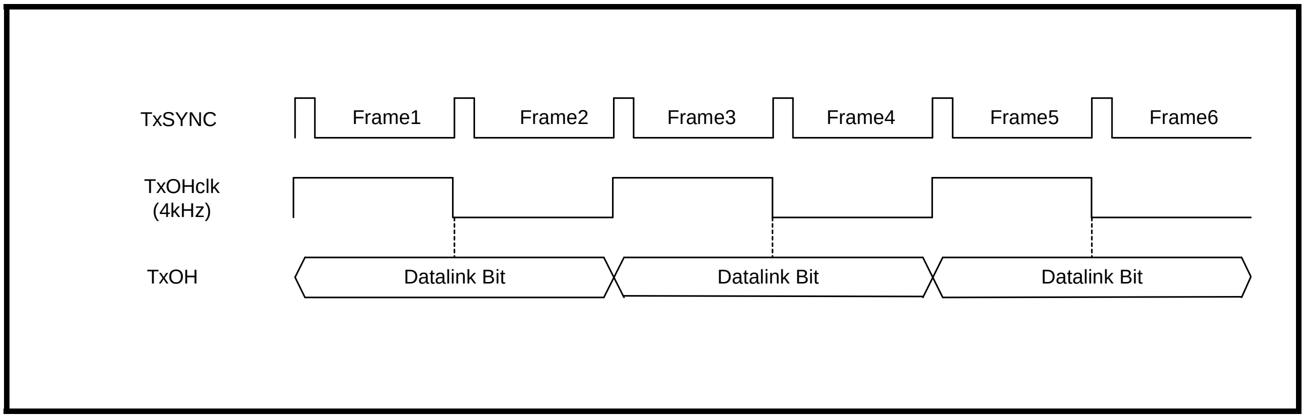
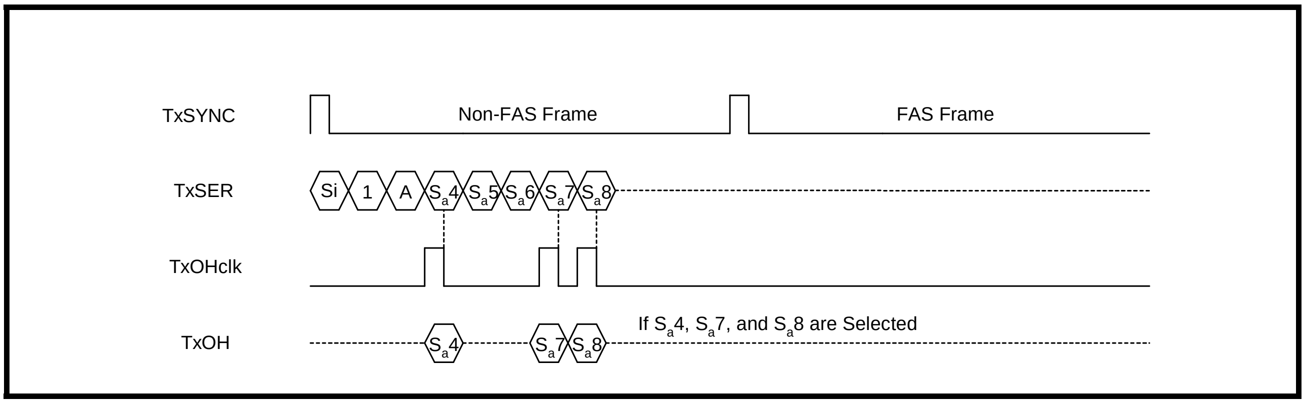


FIGURE 12. E1 OVERHEAD EXTERNAL DATALINK BUS



1.7 High-Speed Non-Multiplexed Interface

The speed of transferring data through a back plane interface in a non-multiplexed manner typically operates at 1.544Mbps, 2.048Mbps, 4.096Mbps, or 8.192Mbps. For 12.352Mbps and 16.384Mbps, see the High-Speed Multiplexed Section. The T1/E1 carrier signal out to or in from the line interface is always 1.544MHz and 2.048MHz respectively. However, the back plane interface may be synchronous to a "Higher" speed clock. For T1, as shown in **Figure 13**, is mapped into an E1 frame. Therefore, every fourth time slot contains non-valid data. For E1, as shown in **Figure 14**, is simply synchronized to the "Higher" 8.192MHz clock signal supplied to the TxMSYNC input pin.

FIGURE 13. T1 HIGH-SPEED NON-MULTIPLEXED INTERFACE

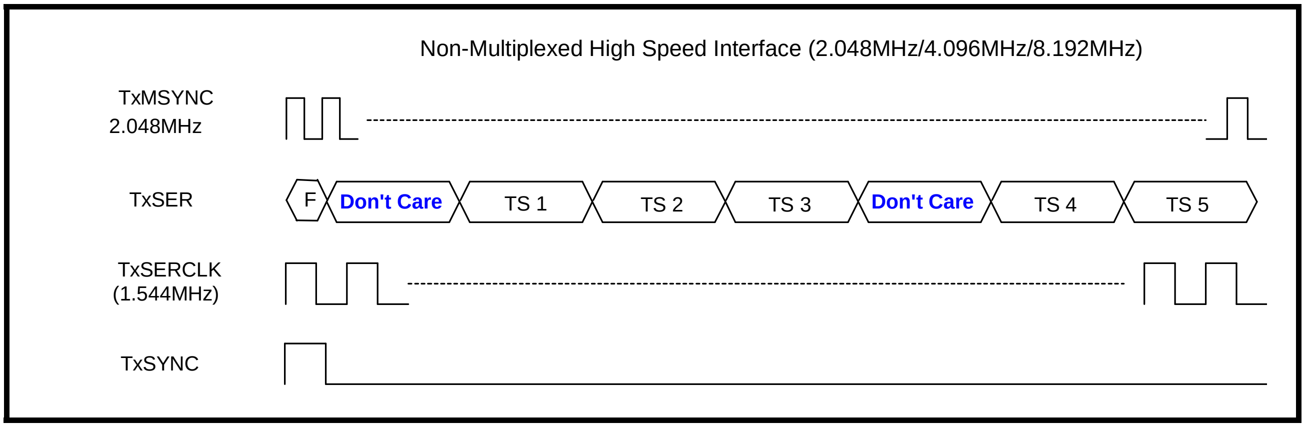
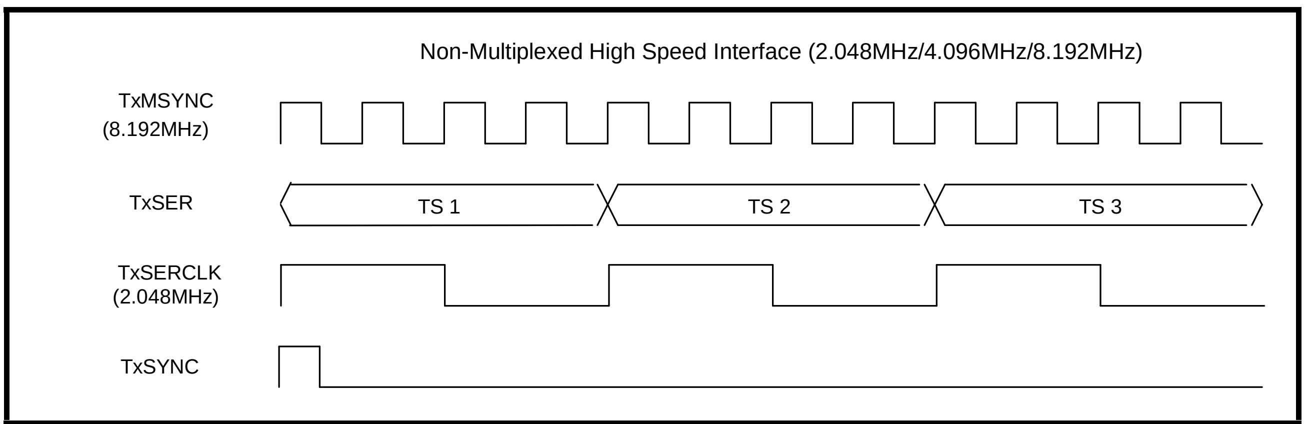


FIGURE 14. E1 HIGH-SPEED NON-MULTIPLEXED INTERFACE



1.8 High-Speed Multiplexed Interface

In addition to the non-multiplexed mode, the framer can interface through the backplane in a high-speed multiplexed application, either through a bit-muxed or byte-muxed (in HMVIP or H.100) manner. In this mode, the chip is divided into two multiplexed blocks, four channels per block. For T1, the high speed multiplexed modes are 12.352Mbps (bit-muxed, TxSYNC is “High” during the F-bit), 16.384Mbps (bit-muxed, TxSYNC is “High” during the F-bit), 16.384Mbps (HMVIP: byte-muxed, TxSYNC is “High” during the last 2-bits of the previous frame and the first 2-bits of the current frame), or 16.384Mbps (H.100: byte-muxed, TxSYNC is “High” during the last bit of the previous frame and the first bit in the current frame). For E1 mode, the only mode that is not supported is the 12.352Mbps. The only other difference is that the F-bit (for T1 mode) becomes the first bit of the E1 frame. **Figure 15** is a simplified block diagram of transmit bit-muxed application. **Figure 16** is a simplified block diagram of receive bit-muxed application. Although the data is only applied to channel 4 or channel 0, the TxSERCLK is necessary for all channels so that the transmit line rate is always equal to the T1/E1 carrier rate.

FIGURE 15. TRANSMIT HIGH-SPEED BIT MULTIPLEXED BLOCK DIAGRAM

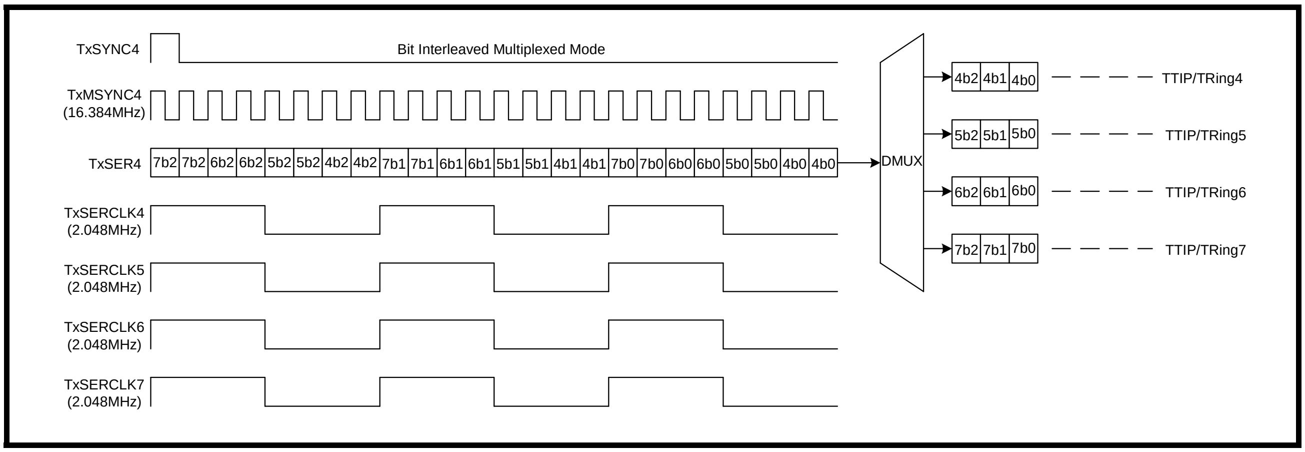


FIGURE 16. RECEIVE HIGH-SPEED BIT MULTIPLEXED BLOCK DIAGRAM