XRP7724

Register Definition Application Note

Table of Contents

1 Introduction 4
2 Register Definitions 5
2.1 Firmware Registers 5
2.2 Voltage Level Configuration Registers 9
2.2.1 Normal and Standby Voltage Levels Registers 9
2.2.2 Voltage Change Threshold Levels Registers 9
2.2.3 Current Change Threshold Levels Registers 10
2.2.4 Supply Voltage Change Control Registers 10
2.3 OVS Registers 10
2.4 PFM Registers 12
2.5 Active Shutdown Threshold Registers 16
2.6 Power Good Registers 16
2.6.1 Power Good Threshold Max Calculation 17
2.3.1 Power Good Threshold Min Calculation 17
2.5 OVP Registers 18
2.5.1 OVP Threshold Calculation 18
2.4 OCP Warning and Fault Registers 19
2.4.1 OCP Calculation 19
2.5 Ramp Continue Threshold Registers 20
2.6 Predefined VIN Registers 20
2.7 Phase Positioning Registers 21
2.8 Current Sample Positioning Registers 21
2.9 OVS Sample Positioning Registers 21
2.10 PWM Configuration Registers 22
2.10.1 PWM Max Duty Ratio Register 22
2.10.2 PWM Min Duty Ratio Register 22
2.10.3 PWM Configuration Register 1 23
2.10.4 PWM Configuration Register 2 23
2.10.5 Dead Time Control Registers 24
2.11 Saturation Limit Register 24
2.12 Target Voltage Setting Register 24
2.13 Ramp Up/Down Setting Registers 25
2.13.1 Ramp Up/Down Calculations 25
2.14 PID Configuration Registers 25
2.14.1 PID Coefficients Registers 26
2.14.2 PID Gain, Scaler, PFM and OVS Enable Registers 27

2.14.3 Zero Error Bin Shift, PID Ramp Gain Registers . . . 27
2.15 Non-linear Encoding, Temperature Sampling, Median Filter Bypass Register . . . 27
2.16 Fault Following Registers . . . 28
2.17 Over Temperature Protection (OTP) Warning, Fault Thresholds and Thermal Restart Registers . . . 28
2.18 Under Voltage Lockout (UVLO) Warning, Fault Thresholds Registers . . . 29
2.19 External Driver Mode Registers . . . 29
2.20 VIN Selector Registers . . . 30
2.21 Fundamental Frequency and Frequency Multipliers Registers . . . 30
2.22 VIN, Temperature Sample Positioning Registers . . . 30
2.23 ADC Configuration Registers . . . 31
2.23.1 Feedback ADC Sampling Time Registers . . . 31
2.23.2 Auxiliary ADC Sampling Time Registers . . . 31
2.23.3 Force Duty Ratio Registers . . . 31
2.23.4 Bypass Sigma Delta, Force Duty Mode Registers . . . 31
2.23.5 Auxiliary ADC VOUT Sampling Time Registers . . . 32
2.23.6 Auxiliary ADC Sampling Time Registers . . . 32
2.23.7 Auxiliary ADC VOUT Sampling Time Register . . . 32
2.24 General Control 1 Registers . . . 33
2.25 PFM Target Registers . . . 33
2.26 General Control 2 Registers . . . 33
2.27 Clock Control Registers . . . 34
2.27.1 Clock Control Register 0 . . . 35
2.27.2 Clock Control Register 1 . . . 36
2.27.3 Clock Control Register 2 . . . 37
2.27.4 External Clock Mode Registers . . . 38
2.28 Boost Feedback Control . . . 39
2.29 Control Registers . . . 39
2.30 I/O Configuration Registers . . . 40
2.30.1 I/O Clock Wake Up Control . . . 40
2.30.2 I/O Control Registers . . . 40
2.31 Special Function Registers . . . 41
2.32 Monitoring Registers . . . 46

1 Introduction

This document provides the register definitions for the XRP7724 device. The register description includes the hardware address to access the register during run-time as well as its Flash address to access the register during configuration.

Unless otherwise noted, the following conditions apply to all XRP7724 registers.

- All bits are active high
- All register fields are R/W
- All registers are 1 byte wide
- Do not read/write to/from reserved registers. Writing to a reserved register will be ignored. Likewise, read a reserved register will return all zeros.

For the majority of users, the GUI should be sufficient for configuring the XRP7724 device. This document is intended for advanced users who wish to modify the XRP7724 settings during runtime. Please contact Exar Technical Support for additional guidance.

2 Register Definitions

2.1 Firmware Registers

This section defines the firmware registers that may be programmed by the user.

Runtime Address	Flash Address	Name	Bits	Description
8072	180	RESERVED	7:0	
8073	181	RUNTIMEBITMAP[7:0]	0	RUN_TIME_RESET_HSI_ON_ZEROS
			1	RUN_TIME_TEST_CMD_ENABLE
			2	RUN_TIME_YF_WRITE_PROTECT
			3	RUN_TIME_RESERVED3
			4	RUN_TIME_PANIC_SHUTDOWN
			5	RUN_TIME_HSI_TIMEOUT_DISABLE
			6	RUN_TIME_ENABLE_GPIO_ON_RSTO_DEASSERT
			7	RUN_TIME_PWREN_CHECK
8074	182	I2CSADDR[7:0]	7:0	8-bit address. Corresponds to 7-bit address 0x28
8075	183	CONFIGVERSION[7:0]	7:0	Configuration Version. Used by the GUI to define the user defined configuration version.
8076	184	PWREN0[7:0]	7:0	Index into sequencer table for Group 0.
8077	185	PWREN1[7:0]	7:0	Index into sequencer table for Group 1.
8078	186	PWREN2[7:0]	7:0	Index into sequencer table for Group 2.
8079	187	PWRENSEQUPDATA_0_DELAY[7:0]	7:0	Start up delay in ms.
807A	188	PWRENSEQUPDATA_0_SEQ[7:0]	7:0	Power up sequence for supplies.
807B	189	PWRENSEQUPDATA_1_DELAY[7:0]	7:0	Start up delay in ms.
807C	18A	PWRENSEQUPDATA_1_SEQ[7:0]	7:0	Power up sequence for supplies.
807D	18B	PWRENSEQUPDATA_2_DELAY[7:0]	7:0	Start up delay in ms.
807E	18C	PWRENSEQUPDATA_2_SEQ[7:0]	7:0	Power up sequence for supplies.
807F	18D	PWRENSEQUPDATA_3_DELAY[7:0]	7:0	Start up delay in ms.
8080	18E	PWRENSEQUPDATA_3_SEQ[7:0]	7:0	Power up sequence for supplies.
8081	18F	PWRENSEQUPDATA_4_DELAY[7:0]	7:0	Start up delay in ms.
8082	190	PWRENSEQUPDATA_4_SEQ[7:0]	7:0	Power up sequence for supplies.
8083	191	PWRENSEQUPDATA_5_DELAY[7:0]	7:0	Start up delay in ms.
8084	192	PWRENSEQUPDATA_5_SEQ[7:0]	7:0	Power up sequence for supplies.
8085	193	PWRENSEQDOWNDATA_0_DELAY[7:0]	7:0	Shut down delay in ms.
8086	194	PWRENSEQDOWNDATA_0_SEQ[7:0]	7:0	Power down sequence for supplies.
8087	195	PWRENSEQDOWNDATA_1_DELAY[7:0]	7:0	Shut down delay in ms.
8088	196	PWRENSEQDOWNDATA_1_SEQ[7:0]	7:0	Power down sequence for supplies.
8089	197	PWRENSEQDOWNDATA_2_DELAY[7:0]	7:0	Shut down delay in ms.
808A	198	PWRENSEQDOWNDATA_2_SEQ[7:0]	7:0	Power down sequence for supplies.
808B	199	PWRENSEQDOWNDATA_3_DELAY[7:0]	7:0	Shut down delay in ms.
808C	19A	PWRENSEQDOWNDATA_3_SEQ[7:0]	7:0	Power down sequence for supplies.
808D	19B	PWRENSEQDOWNDATA_4_DELAY[7:0]	7:0	Shut down delay in ms.
808E	19C	PWRENSEQDOWNDATA_4_SEQ[7:0]	7:0	Power down sequence [39:32] for supplies.
808F	19D	PWRENSEQDOWNDATA_5_DELAY[7:0]	7:0	Shut down delay [47:40] in ms.
8090	19E	PWRENSEQDOWNDATA_5_SEQ[7:0]	7:0	Power down sequence [47:40] for supplies.
8091	19F	SUPSEQ_FAULTDELAY_CH0[7:0]	7:0	Start up Timeout: time to wait in ms for Channel 1 to enable.
8092	1A0	SUPSEQ_CFG_CH0[7:0]	7:0	Sequencer configuration data.

Runtime Address	Flash Address	Name	Bits	Description
8093	1A1	SUPSEQ_VOUTDELAY_CH0[7:0]	7:0	Sequencer delay data .
8094	1A2	SUPSEQ_RESTARTDELAY_CH0 [7:0]	7:0	Channel 1 Hiccup Timeout. Time in ms to delay before Channel 1 restarts.
8095	1A3	SUPSEQ_FAULTDELAY_CH01[7:0]	7:0	Start up Timeout: time to wait in ms for Channel 2 to enable .
8096	1A4	SUPSEQ_CFG_CH1[7:0]	7:0	Sequencer configuration data.
8097	1A5	SUPSEQ_VOUTDELAY_CH1[7:0]	7:0	Sequencer delay data
8098	1A6	SUPSEQ_RESTARTDELAY_CH1[7:0]	7:0	Channel 2 Hiccup Timeout. Time in ms to delay before Channel 2 restarts.
8099	1A7	SUPSEQ_FAULTDELAY_CH02[7:0]	7:0	Start up Timeout: time to wait in ms for Channel 3 to enable.
809A	1A8	SUPSEQ_CFG_CH2[7:0]	7:0	Sequencer configuration data.
809B	1A9	SUPSEQ_VOUTDELAY_CH2[7:0]	7:0	Sequencer delay data.
809C	1AA	SUPSEQ_RESTARTDELAY_CH2[7:0]	7:0	Channel 3 Hiccup Timeout. Time in ms to delay before Channel 3 restarts.
809D	1AB	SUPSEQ_FAULTDELAY_CH03[7:0]	7:0	Start up Timeout: time to wait in ms for Channel 4 to enable
809E	1AC	SUPSEQ_CFG_CH3[7:0]	7:0	Sequencer configuration data
809F	1AD	SUPSEQ_VOUTDELAY_CH3[7:0]	7:0	Sequencer delay data
80A0	1AE	SUPSEQ_RESTARTDELAY_CH3[7:0]	7:0	Channel 4 Hiccup Timeout. Time in ms to delay before Channel 4 restarts.
80A1	1AF	RESERVED		
80A2	1B0	SUPSEQ_CFG_CH4[7:0]	7:0	Sequencer configuration data.
80A3	1B1	SUPSEQ_VOUTDELAY_CH4[7:0]	7:0	Sequencer delay data.
80A4	1B2	RESERVED		
80A5	1B3	HSITIMERRELOAD[7:0]	7:0	HSI Reset timer in ms. Default 0x19 (25ms).
80A6	1B4	FW_GPIO0[7:0]	7:0	GPIO0 Input Configuration. 0x00 GPIO_GENERAL_INPUT 0x01 GPIO_PWREN1 Group 1 enable 0x02 GPIO_PWREN2 Group 2 enable 0x03 GPIO_CHEN0 Channel 1 enable 0x04 GPIO_CHEN1 Channel 2 enable 0x05 GPIO_CHEN2 Channel 3 enable 0x06 GPIO_CHEN3 Channel 4 enable 0x07 GPIO_LDO3.3_EN LDO3.3 enable 0x08 RESERVED 0x09 GPIO_SUPPLY_NORM_STDBY 0x0A GPIO_I2C_ADDR_LSB requires SET_GPIO0_CFG = 0x61

Runtime Address	Flash Address	Name	Bits	Description
80A7	1B5	FW_GPIO1[7:0]	7:0	GPIO1 Input Configuration. 0x00 GPIO_GENERAL_INPUT 0x01 GPIO_PWREN1 Group 1 enable 0x02 GPIO_PWREN2 Group 2 enable 0x03 GPIO_CHEN0 Channel 1 enable 0x04 GPIO_CHEN1 Channel 2 enable 0x05 GPIO_CHEN2 Channel 3 enable 0x06 GPIO_CHEN3 Channel 4 enable 0x07 GPIO_LDO3.3_EN LDO3.3 enable 0x08 RESERVED 0x09 GPIO_SUPPLY_NORM_STDBY 0x0A GPIO_I2C_ADDR_LSB requires SET_GPIO0_CFG = 0x61)
80A8	1B6	FW_GPIO2[7:0]	7:0	PSIO0 Input Configuration. 0x00 GPIO_GENERAL_INPUT 0x01 GPIO_PWREN1 Group 1 enable 0x02 GPIO_PWREN2 Group 2 enable 0x03 GPIO_CHEN0 Channel 1 enable 0x04 GPIO_CHEN1 Channel 2 enable 0x05 GPIO_CHEN2 Channel 3 enable 0x06 GPIO_CHEN3 Channel 4 enable 0x07 GPIO_LDO3.3_EN LDO3.3 enable 0x08 RESERVED 0x09 GPIO_SUPPLY_NORM_STDBY 0x0A GPIO_I2C_ADDR_LSB requires SET_GPIO0_CFG = 0x61
80A9	1B7	FW_GPIO3[7:0]	7:0	PSIO1 Input Configuration 0x00 GPIO_GENERAL_INPUT 0x01 GPIO_PWREN1 – Group 1 enable 0x02 GPIO_PWREN2 – Group 2 enable 0x03 GPIO_CHEN0 – Channel 1 enable 0x04 GPIO_CHEN1 – Channel 2 enable 0x05 GPIO_CHEN2 – Channel 3 enable 0x06 GPIO_CHEN3 – Channel 4 enable 0x07 GPIO_LDO3.3_EN – LDO3.3 enable 0x08 RESERVED 0x09 GPIO_SUPPLY_NORM_STDBY 0x0A GPIO_I2C_ADDR_LSB (requires SET_GPIO0_CFG = 0x61)

Runtime Address	Flash Address	Name	Bits	Description
80AA	1B8	FW_GPIO4[7:0]	7:0	PSIO2 Input Configuration. 0x00 GPIO_GENERAL_INPUT 0x01 GPIO_PWREN1 Group 1 enable 0x02 GPIO_PWREN2 Group 2 enable 0x03 GPIO_CHEN0 Channel 1 enable 0x04 GPIO_CHEN1 Channel 2 enable 0x05 GPIO_CHEN2 Channel 3 enable 0x06 GPIO_CHEN3 Channel 4 enable 0x07 GPIO_LDO3.3_EN – LDO3.3 enable 0x08 RESERVED 0x09 GPIO_SUPPLY_NORM_STDBY 0x0A GPIO_I2C_ADDR_LSB (requires SET_GPIO0_CFG = 0x61)
80AB	1B9	GPIO_POK_CFG[7:0]	7:0	I/O Power OK Output Pin Select. 0x00 GPIO0 0x01 GPIO1 0x02 PSIO0 0x03 PSIO1 0x04 PSIO2
80AC	1BA	GPIO_RSTO_CFG[7:0]	7:0	I/O Reset Out Output Pin Select. 0x00 GPIO0 0x01 GPIO1 0x02 PSIO0 0x03 PSIO1 0x04 PSIO2
80AD	1BB	TRSTO_CFG[7:0]	7:0	Reset Out Delay Configuration. 5ms per LSB
80AE	1BC	AUXBITMAP[7:0]	7:0	0x00 AUX_DISABLE_UVLO_F_CHK_IN_250MS 0x01 AUX_DISABLE_UVLO_W_CHK_IN_250MS 0x02 AUX_RESET_ON_UVLO_CLEAR 0x03 AUX_FORCE_250MS_OTP_READ
80AF	1BD	GPIO_LOWVIN[7:0]	7:0	LOW_VIN Output Pin Select. 0x00 GPIO0 0x01 GPIO1 0x02 PSIO0 0x03 PSIO1 0x04 PSIO2
80B0	1BE	GPIO_INTR[7:0]	7:0	INTR Output Pin Select. 0x00 GPIO0 0x01 GPIO1 0x02 PSIO0 0x03 PSIO1 0x04 PSIO2

2.2 Voltage Level Configuration Registers

This section defines the registers used to configure the target voltage levels.

2.2.1 Normal and Standby Voltage Levels Registers

This section defines the registers used to program the normal and standby voltage levels for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
80B1	11F	SUPPLYVTAR_CH0[7:0]	7:0	Channel 1 Normal target voltage in native resolution set in GUI..
80B2	120	SUPPLYVTAR_CH1[7:0]	7:0	Channel 2 Normal target voltage in native resolution set in GUI.
80B3	121	SUPPLYVTAR_CH2[7:0]	7:0	Channel 3 Normal target voltage in native resolution set in GUI.
80B4	122	SUPPLYVTAR_CH3[7:0]	7:0	Channel 4 Normal target voltage in native resolution set in GUI.
80B5	123	SUPPLYVTARSTBY_CH0[7:0]	7:0	Channel 1 Standby target voltage in native resolution. Default 0.6V.
80B6	124	SUPPLYVTARSTBY_CH1[7:0]	7:0	Channel 2 Standby target voltage in native resolution. Default 0.6V.
80B7	125	SUPPLYVTARSTBY_CH2[7:0]	7:0	Channel 3 Standby target voltage in native resolution. Default 0.6V.
80B8	126	SUPPLYVTARSTBY_CH3[7:0]	7:0	Channel 4 Standby target voltage in native resolution. Default 0.6V.

2.2.2 Voltage Change Threshold Levels Registers

This section defines the registers used to program the minimum and maximum voltage thresholds for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
80B9	127	PWRSETVOLTAGETHRESHMIN_CH0_LOW[7:0]	7:0	Minimum voltage set value through HSI for Channel 1. Default 0x00.
80BA	128	PWRSETVOLTAGETHRESHMIN_CH0_HIGH[7:0]	7:0	Minimum voltage set value through HSI for Channel 1. Default 0x00.
80BB	129	PWRSETVOLTAGETHRESHMIN_CH1_LOW[7:0]	7:0	Minimum voltage set value through HSI for Channel 2. Default 0x00.
80BC	12A	PWRSETVOLTAGETHRESHMIN_CH1_HIGH[7:0]	7:0	Minimum voltage set value through HSI for Channel 2. Default 0x00.
80BD	12B	PWRSETVOLTAGETHRESHMIN_CH2_LOW[7:0]	7:0	Minimum voltage set value through HSI for Channel 3. Default 0x00.
80BE	12C	PWRSETVOLTAGETHRESHMIN_CH2_HIGH[7:0]	7:0	Minimum voltage set value through HSI for Channel 3. Default 0x00.
80BF	12D	PWRSETVOLTAGETHRESHMIN_CH3_LOW[7:0]	7:0	Minimum voltage set value through HSI for Channel 4. Default 0x00.
80C0	12E	PWRSETVOLTAGETHRESHMIN_CH3_HIGH[7:0]	7:0	Minimum voltage set value through HSI for Channel 4. Default 0x00.
80C1	12F	PWRSETVOLTAGETHRESHMAX_CH0_LOW[7:0]	7:0	Maximum voltage set value through HSI for Channel 1. Default 0xFF.
80C2	130	PWRSETVOLTAGETHRESHMAX_CH0_HIGH[7:0]	7:0	Maximum voltage set value through HSI for Channel 1. Default 0xFF.
80C3	131	PWRSETVOLTAGETHRESHMAX_CH1_LOW[7:0]	7:0	Maximum voltage set value through HSI for Channel 2. Default 0xFF.
80C4	132	PWRSETVOLTAGETHRESHMAX_CH1_HIGH[7:0]	7:0	Maximum voltage set value through HSI for Channel 2. Default 0xFF.
80C5	133	PWRSETVOLTAGETHRESHMAX_CH2_LOW[7:0]	7:0	Maximum voltage set value through HSI for Channel 3. Default 0xFF.

Runtime Address	Flash Address	Name	Bits	Description
80C6	134	PWRSETVOLTAGETHRESHMAX_CH2_HIGH[7:0]	7:0	Maximum voltage set value through HSI for Channel 3. Default 0xFF.
80C7	135	PWRSETVOLTAGETHRESHMAX_CH3_LOW[7:0]	7:0	Maximum voltage set value through HSI for Channel 4. Default 0xFF.
80C8	136	PWRSETVOLTAGETHRESHMAX_CH3_HIGH[7:0]	7:0	Maximum voltage set value through HSI for Channel 4. Default 0xFF.

2.2.3 Current Change Threshold Levels Registers

This section defines the registers used to program the minimum and maximum current thresholds for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
80C9	137	PWRSETCURRENTTHRESHMAX_CH0[7:0]	7:0	Max current set value through HSI Channel 1. Default 0xFF.
80CA	138	PWRSETCURRENTTHRESHMAX_CH1[7:0]	7:0	Max current set value through HSI Channel 2. Default 0xFF.
80CB	139	PWRSETCURRENTTHRESHMAX_CH2[7:0]	7:0	Max current set value through HSI Channel 3. Default 0xFF.
80CC	13A	PWRSETCURRENTTHRESHMAX_CH3[7:0]	7:0	Max current set value through HSI Channel 4. Default 0xFF.

2.2.4 Supply Voltage Change Control Registers

This section defines the register used to enable each channel's behavior as it transitions from normal to standby. Setting the channel number bit will cause that channel to transition into standby when appropriate, otherwise the channel will remain in normal mode.

Runtime Address	Flash Address	Name	Bits	Description
80CD	13B	SUPPLYGPIONORMSTBYCFG[3:0]	7:0	Bitwise control of which channel will transition between normal and standby from an I/O (if configured). Bit 0 Channel 1 Bit 1 Channel 2 Bit 2 Channel 3 Bit 3 Channel 4
80CE	13C	RESERVED	7:0	
80CF	13D	RESERVED	7:0	
80D0	13E	RESERVED	7:0	

2.3 OVS Registers

This section defines the registers used to program the OVS properties for channels 1-4.

Run time Address	Flash Address	Name	Bits	Description
C000	000	STA_OVS_DUTY_SAT_CH0[7:0]	7:0	OVS Duty Saturation. If OVS duty is greater than this value, hold the high-side on until the end of the quarter cycle (or sampling period). Each bit represents one counter step of the 103MHz clock. Percentage of counter_restart_state/4 (50-90%)
C100	040	STA_OVS_DUTY_SAT_CH1[7:0]	7:0	
C200	080	STA_OVS_DUTY_SAT_CH2[7:0]	7:0	
C300	0C0	STA_OVS_DUTY_SAT_CH3[7:0]	7:0	

Run time Address	Flash Address	Name	Bits	Description
C001 C101 C201 C301	001 041 081 0C1	STA_OVS_LS_CUR_CH0[7:0] STA_OVS_LS_CUR_CH1[7:0] STA_OVS_LS_CUR_CH2[7:0] STA_OVS_LS_CUR_CH3[7:0]	5:0	Low Side Current Measure. Indicates when the low-side should be turned on in the last 1/16th of the switching cycle, in system clock cycles. Dead-time will decrease the effective on-time of the low side switching signal. Each bit represents one counter step of the 103MHz clock. The value should be large enough to ensure one ADC sample and hold action for the current measurement. Set to ((counter_restart_state + 1) / 16) - 1
			6	U-OVS Dead Time Safe Mode. When set, dead-time will always occur during a transition to U-OVS mode.
			7	U-OVS First Pulse Limit. If set, ovs_first_pulse_max will be used to limit the size of the first pulse upon entering u_ovs mode.
C002	002	STA_OVS_INIT_OFFTIME_CH0[7:0]	7:0	OVS Initial Off Time. In O_OVS mode, set both HS and LS signals off at the beginning before turning LS on. Units are system clock cycles. One bit represents one counter step of the 103MHz clock.
C102	042	STA_OVS_INIT_OFFTIME_CH1[7:0]	7:0	
C202	082	STA_OVS_INIT_OFFTIME_CH2[7:0]	7:0	
C302	0C2	STA_OVS_INIT_OFFTIME_CH3[7:0]	7:0	
C003 C103 C203 C301	003 043 083 0C3	STA_OVS_ESR_DEADTIME_CH0[7:0] STA_OVS_ESR_DEADTIME_CH1[7:0] STA_OVS_ESR_DEADTIME_CH2[7:0] STA_OVS_ESR_DEADTIME_CH3[7:0]	1:0	Large ESR Mode. Indicates whether the capacitor has large or small ESR. Relevant only during U_OVS mode. If ESR is small, the OVS high-side switching signal is OR'ed with the DPWM signal to produce the final signal. If the ESR is large, the DPWM high-side signal is ignored during U_OVS mode. 10 small ESR 01 large ESR 00/11 middle range ESR If C_ESR > 5Mohm, set to 2'b01; if C_ESR < 5Mohm, set to 2'b10.
			7:2	Course Dead Time. Dead-time in system clock cycles. At the beginning of U_OVS mode, wait this amount of time before turning on the high-side. In either O_OVS mode or U_OVS mode in the last 1/16th of each switching period, wait this amount of time with both LS and HS off before using PID switching signals to always ensure dead-time requirements are met. Each bit represents one counter step with the 25MHz clock. Calculated to be equal to dead_time_hs_0 / 32.
C017 C117 C217 C317	017 057 097 0D7	STA_PGOOD_THRES_UPPER_CH0[7:0] STA_PGOOD_THRES_UPPER_CH1[7:0] STA_PGOOD_THRES_UPPER_CH2[7:0] STA_PGOOD_THRES_UPPER_CH3[7:0]	0	Maximum Error Threshold. Bit 8 of Power Good upper threshold
			1	Minimum Error Threshold. Bit 8 of Power Good upper threshold
			2]	PFM to PWM Error. Initial error value upon PFM-->PWM transition should correspond to comparator reference Each bit represents one step in the encoded 9 bit error signal.
			7:3	U-OVS First Pulse Maximum. When we enter under voltage OVS mode, limit the first pulse to this duty ratio if u_ovs_first_pulse_limit is set high (each bit is 8 103 MHz clock cycles). Percentage of counter_restart_state/8 (50-90%).

Run time Address	Flash Address	Name	Bits	Description
C030	030	DYN_OVS_K_UPPER_CH0[6:0]	14:8	OVS Controller Gain[14:0].
C030	031	DYN_OVS_K_LOWER_CH0[7:0]	7:0	
C130	070	DYN_OVS_K_UPPER_CH1[6:0]	14:8	
C131	071	DYN_OVS_K_LOWER_CH1[7:0]	7:0	
C230	0B0	DYN_OVS_K_UPPER_CH2[6:0]	14:8	
C231	0B1	DYN_OVS_K_LOWER_CH2[7:0]	7:0	
C330	0F0	DYN_OVS_K_UPPER_CH3[6:0]	14:8	
C331	0F1	DYN_OVS_K_LOWER_CH3[7:0]	7:0	

2.4 PFM Registers

This section defines the registers used to program the PFM related characteristics for channels 1-4.

Run time Address	Flash Address	Name	Bits	Description
C004 C104 C204 C304	004 044 084 0C4	STA_PFM_T_MAX_UPPER_CH0[7:0] STA_PFM_T_MAX_UPPER_CH1[7:0] STA_PFM_T_MAX_UPPER_CH2[7:0] STA_PFM_T_MAX_UPPER_CH3[7:0]	11:8	Maximum Switching Period. The maximum desired switching period, in ring_clk periods. Assuming a ring_clk frequency of 103MHz and a maximum desired switching frequency of 100kHz, this value would be set to 103MHz / 100kHz = d1030 clock periods.
			7:4	Sigma Delta Data PFM Offset[7:4]. An offset to add or subtract from sigma_delta_data before it's sent to the DPWM. sign and magnitude representation - when the MSB is 1 it is a negative number (sigma_delta_data_out is reduced). This register is split between Cx04 [7:4] and Cx06 [7:4].
C005	005	STA_PFM_T_MAX_LOWER_CH0[7:0]	7:0	PFM Target Maximum[7:0]. The maximum desired switching period, in ring_clk periods. Assuming a ring_clk frequency of 103MHz and a maximum desired switching frequency of 100kHz, this value would be set to 103MHz / 100kHz = d1030 clock periods.
C105	045	STA_PFM_T_MAX_LOWER_CH1[7:0]	7:0	
C205	085	STA_PFM_T_MAX_LOWER_CH2[7:0]	7:0	
C305	0C5	STA_PFM_T_MAX_LOWER_CH3[7:0]	7:0	
C006 C106 C206 C306	006 046 086 0C6	STA_PFM_T_MIN_UPPER_CH0[7:0] STA_PFM_T_MIN_UPPER_CH1[7:0] STA_PFM_T_MIN_UPPER_CH2[7:0] STA_PFM_T_MIN_UPPER_CH3[7:0]	3:0	PFM Target Minimum[11:8]. The minimum desired switching period, in ring_clk periods. Assuming a ring_clk frequency of 100MHz and a minimum desired switching frequency of 100kHz, this value would be set to 103MHz / 30kHz = d3433 clock periods. This value is also the fixed switching period that is used in Ultrasonic Mode.
			7:4	Sigma Delta Data PFM Offset[3:0]. An offset to add or subtract from sigma_delta_data before it's sent to the DPWM. sign and magnitude representation - when the MSB is 1 it is a negative number (sigma_delta_data_out is reduced). This register is split between Cx04 [7:4] and Cx06 [7:4].
C007	007	STA_PFM_T_MIN_LOWER_CH0[7:0]	7:0	PFM Target Minimum. The minimum desired switching period, in ring_clk periods. Assuming a ring_clk frequency of 100MHz and a minimum desired switching frequency of 100kHz, this value would be set to 103MHz / 30kHz = d3433 clock periods. This value is also the fixed switching period that is used in Ultrasonic Mode.
C107	047	STA_PFM_T_MIN_LOWER_CH1[7:0]	7:0	
C207	087	STA_PFM_T_MIN_LOWER_CH2[7:0]	7:0	
C307	0C7	STA_PFM_T_MIN_LOWER_CH3[7:0]	7:0	

Run time Address	Flash Address	Name	Bits	Description
C008 C108 C208 C308	008 048 088 0C8	STA_PFM_K_MAX_MIN_UPPER_CH0[7:0] STA_PFM_K_MAX_MIN_UPPER_CH1[7:0] STA_PFM_K_MAX_MIN_UPPER_CH2[7:0] STA_PFM_K_MAX_MIN_UPPER_CH3[7:0]	0	PFM_K_MAX[8]. Corresponds to how much the alive-time should be multiplied by when the previous switching period was too large. The MSB is an integer and the 8 LSB's are decimal values. This value should be slightly less than one (MSB = 0) in order to decrease the alive time. PFM_K_MAX set to fixed value: 0x00DA.
			1	PFM_K_MIN[8]. Corresponds to how much the alive-time should be multiplied by when the previous switching period was too small. The MSB is an integer and the 8 LSB's are decimal values. his value should be slightly greater than one (MSB = 0) in order to increase the alive time. PFM_K_MIN set to fixed value: 0x0120.
C009	009	STA_PFM_K_MAX_LOWER_CH0[7:0]	7:0	PFM_K_MAX[7:0]. Corresponds to how much the alive-time should be multiplied by when the previous switching period was too large. The MSB is an integer and the 8 LSB's are decimal values. This value should be slightly less than one (MSB = 0) in order to decrease the alive time. PFM_K_MAX set to fixed value: 0x00DA.
C109	049	STA_PFM_K_MAX_LOWER_CH1[7:0]	7:0	
C209	089	STA_PFM_K_MAX_LOWER_CH2[7:0]	7:0	
C309	0C9	STA_PFM_K_MAX_LOWER_CH3[7:0]	7:0	
C00A	00A	STA_PFM_K_MIN_LOWER_CH0[7:0]	7:0	PFM_K_MIN[7:0]. Corresponds to how much the alive-time should be multiplied by when the previous switching period was too small. The MSB is an integer and the 8 LSB's are decimal values. This value should be slightly greater than one (MSB = 0) in order to increase the alive time. PFM_K_MIN set to fixed value: 0x0120..
C10A	04A	STA_PFM_K_MIN_LOWER_CH1[7:0]	7:0	
C20A	08A	STA_PFM_K_MIN_LOWER_CH2[7:0]	7:0	
C30A	0CA	STA_PFM_K_MIN_LOWER_CH3[7:0]	7:0	
C00D	00D	STA_PFM_ALIVE_MIN_CH0[7:0]	7:0	PFM Alive Min[7:0]. Corresponds to the maximum alive-time value. The alive-time is saturated to this value. Each bit represents 4 counter steps of the 25MHz clock. Default (Fixed) value: 0x20
C10D	04D	STA_PFM_ALIVE_MIN_CH1[7:0]	7:0	
C20D	08D	STA_PFM_ALIVE_MIN_CH2[7:0]	7:0	
C30D	0CD	STA_PFM_ALIVE_MIN_CH3[7:0]	7:0	
C00E	00E	STA_PFM_ALIVE_MAX_CH0[7:0]	7:0	PFM Alive Max[7:0]. Corresponds to the minimum alive-time value. The alive-time is saturated to this value. If the alive-time is saturated to this value and the switching frequency is still too small, then the PFM controller will switch into Ultrasonic Mode. Each bit represents 4 counter steps of the 25MHz clock. Calculated to be equal to channel's counter_restart_state (see Configure PFM function).
C10E	04E	STA_PFM_ALIVE_MAX_CH1[7:0]	7:0	
C20E	08E	STA_PFM_ALIVE_MAX_CH2[7:0]	7:0	
C30E	0CE	STA_PFM_ALIVE_MAX_CH3[7:0]	7:0	

Run time Address	Flash Address	Name	Bits	Description
C00F	00F	STA_PFM_DEAD_ZONE_CH0[7:0]	5:0	PFM Dead Zone. Defines how long to wait after the start of a period before reading the PFM comparator value. This prevents the controller from sending pulses too frequently. In PFM mode, the PFM controller should dictate when switching periods begin. As a result, a low value of pfm_pwm_dead_zone should be sent to the DPWM (for example, a value of 0 or 1). This allows the PFM controller to control the dead zone. Each bit represents 4 counter steps of the 25MHz clock. Calculated to be equal to channel's counter_restart_state /16
C10F	04F	STA_PFM_DEAD_ZONE_CH1[7:0]	5:0	
C20F	08F	STA_PFM_DEAD_ZONE_CH2[7:0]	5:0	
C30F	0CF	STA_PFM_DEAD_ZONE_CH3[7:0]	5:0	
C010 C110 C210 C310	010 050 090 0D0	STA_PFM_ENABLE_CONFIG_CH0[7:0] STA_PFM_ENABLE_CONFIG_CH1[7:0] STA_PFM_ENABLE_CONFIG_CH2[7:0] STA_PFM_ENABLE_CONFIG_CH3[7:0]	0	ULTRASONIC_ENABLE. Enables ltrasonic mode.
			1	FREQUENCY_TARGETING_ENABLE. Enables frequency targeting mode.
			2	FORCE_MIN_FREQ. Forces a pulse when the frequency falls below this limit. Set to "1" if Ultrasonic mode is enabled.
			3	BT_FORCE_ENABLE. Enables brute-force shutdown in OVP.
			4	DRIVER_TEST_SEL. Enables driver test mode for one channel.
C011	011	STA_PFM_ULTRA_INCR_UPPER_CH0[7:0]	3:0	PFM Ultrasonic Increment[11:8]. Specifies how much to increment or decrement the on-time when in Ultrasonic Mode. Each bit represents 1 counter step of the 25MHz clock. Calculated as (pfm_ultrasonic_max - pfm_ultrasonic_min) / 20 with a minimum value of 1.
C111	051	STA_PFM_ULTRA_INCR_UPPER_CH1[7:0]	3:0	
C211	091	STA_PFM_ULTRA_INCR_UPPER_CH2[7:0]	3:0	
C311	0D1	STA_PFM_ULTRA_INCR_UPPER_CH3[7:0]	3:0	
C012	012	STA_PFM_ULTRA_INCR_LOWER_CH0[7:0]	7:0	PFM Ultrasonic Increment[7:0]. Specifies how much to increment or decrement the on-time during Ultrasonic Mode. Each bit represents 1 counter step of the 25MHz clock. Calculated as (pfm_ultrasonic_max - pfm_ultrasonic_min) / 20 with a minimum value of 1.
C112	052	STA_PFM_ULTRA_INCR_LOWER_CH1[7:0]	7:0	
C212	092	STA_PFM_ULTRA_INCR_LOWER_CH2[7:0]	7:0	
C312	0D2	STA_PFM_ULTRA_INCR_LOWER_CH3[7:0]	7:0	
C013	013	STA_PFM_ULTRA_MAX_UPPER_CH0[7:0]	3:0	PFM Ultrasonic Max[11:8]. The minimum on-time during Ultrasonic Mode. The on-time will saturate at this value. The pfm_ultrasonic_min parameter should be larger than pfm_ultrasonic_increment to prevent overflow in the comparison. Each bit represents 1 counter step of the 25MHz clock. Calculated as pfm_alive_time_min * 4 * (Vout / Vin) * 1.2 under the assumption that input voltage will not increase above more than 20% higher than its nominal value.
C113	053	STA_PFM_ULTRA_INCR_LOWER_CH1[7:0]	3:0	
C213	093	STA_PFM_ULTRA_MAX_UPPER_CH2[7:0]	3:0	
C313	0D3	STA_PFM_ULTRA_MAX_UPPER_CH3[7:0]	3:0	

Run time Address	Flash Address	Name	Bits	Description
C013	013	STA_PFM_ULTRA_MAX_LOWER_CH0[7:0]	7:0	PFM Ultrasonic Max[7:0]. The minimum on-time during Ultrasonic Mode. he on-time will saturate at this value. The pfm_ultrasonic_min parameter should be larger than pfm_ultrasonic_increment to prevent overflow in the comparison. Each bit represents 1 counter step of the 25MHz clock. Calculated as pfm_alive_time_min * 4 * (Vout / Vin) * 1.2 under the assumption that input voltage will not increase above more than 20% higher than its nominal value.
C113	053	STA_PFM_ULTRA_MAX_LOWER_CH1[7:0]	7:0	
C213	093	STA_PFM_ULTRA_MAX_LOWER_CH2[7:0]	7:0	
C313	0D3	STA_PFM_ULTRA_MAX_LOWER_CH3[7:0]	7:0	
C015	015	STA_PFM_ULTRA_MIN_UPPER_CH0[7:0]	3:0	PFM Ultrasonic Min[11:8]. The maximum on-time during Ultrasonic Mode. The on-time will saturate at this value. The pfm_ultrasonic_max parameter should be smaller than (14'b0 – pfm_ultrasonic_increment) to prevent overflow in the comparison. Each bit represents 1 counter step of the 25MHz clock. Calculated as pfm_ultrasonic_max * 0.5.
C115	055	STA_PFM_ULTRA_MIN_UPPER_CH1[7:0]	3:0	
C215	095	STA_PFM_ULTRA_MIN_UPPER_CH2[7:0]	3:0	
C315	0D5	STA_PFM_ULTRA_MIN_UPPER_CH3[7:0]	3:0	
C016	016	STA_PFM_ULTRA_MIN_LOWER_CH0[7:0]	7:0	PFM Ultrasonic Min[7:0]. The maximum on-time during Ultrasonic Mode. The on-time will saturate at this value. The pfm_ultrasonic_max parameter should be smaller than (14'b0 – pfm_ultrasonic_increment) to prevent overflow in the comparison. Each bit represents 1 counter step of the 25MHz clock. Calculated as pfm_ultrasonic_max * 0.5.
C116	056	STA_PFM_ULTRA_MIN_LOWER_CH1[7:0]	7:0	
C216	096	STA_PFM_ULTRA_MIN_LOWER_CH2[7:0]	7:0	
C316	0D6	STA_PFM_ULTRA_MIN_LOWER_CH3[7:0]	7:0	
C017 C117 C217 C317	017 057 097 0D7	STA_PGOOD_THRES_UPPER_CH0[7:0] STA_PGOOD_THRES_UPPER_CH1[7:0] STA_PGOOD_THRES_UPPER_CH2[7:0] STA_PGOOD_THRES_UPPER_CH3[7:0]	0	ERROR_THRESH_MAX. Bit 8 of Power Good upper threshold
			1	ERROR_THRESH_MIN. Bit 8 of Power Good upper threshold
			2	PFM2PWM_ERROR. Initial error value upon PFM-->PWM transition should correspond to comparator reference. Each bit represents one step in the encoded 9 bit error signal.
			7:3	U_OVS_FIRST_PULSE_MAX. When we enter under voltage OVS mode, limit the first pulse to this duty ratio if u_ovs_first_pulse_limit is set high (each bit is 8 103 MHz clock cycles). Percentage of counter_restart_state/8 (50-90%).
C01E	01E	STA_PFM_ERR_INIT_LOWER_CH0[7:0]	7:0	Initial error value upon PFM-->PWM transition. Each bit represents one step in the encoded 9 bit error signal. Set = 4 * Vout * (1 - below_comparator_percentage_offset) / (2.5e-3 * 2^prescaler)
C11E	05E	STA_PFM_ERR_INIT_LOWER_CH1[7:0]	7:0	
C21E	09E	STA_PFM_ERR_INIT_LOWER_CH2[7:0]	7:0	
C31E	0DE	STA_PFM_ERR_INIT_LOWER_CH3[7:0]	7:0	

Run time Address	Flash Address	Name	Bits	Description
C025	025	STA_PFM_I_THRES_CH0[7:0]	5:0	Current threshold to start PFM mode. Same resolution as current samples, each bit represents 1 step in AUX ADC output, or 0.0025V per step (offset 0.04V) with 4x IFE scale and 0.00125V per step (offset 0.02V) with 8x IFE scale.
C125	065	STA_PFM_I_THRES_CH1[7:0]	5:0	
C225	0A5	STA_PFM_I_THRES_CH2[7:0]	5:0	
C325	0E5	STA_PFM_I_THRES_CH3[7:0]	5:0	
C026	026	STA_PFM_DETECTION_TIME_CH0[7:0]	5:0	PFM condition needs to be met for this many cycle to enter the PFM mode. Number of switching cycles, from 0 to 63.
C126	066	STA_PFM_DETECTION_TIME_CH1[7:0]	5:0	
C226	0A6	STA_PFM_DETECTION_TIME_CH2[7:0]	5:0	
C326	0E6	STA_PFM_DETECTION_TIME_CH3[7:0]	5:0	

2.5 Active Shutdown Threshold Registers

This section defines the register used to program the minimum voltage threshold below which the device will shutdown.

Runtime Address	Flash Address	Name	Bits	Description
C00B	00B	STA_SHTDN_STOP_THRESH_CH0[7:0]	7:0	Active Shutdown Threshold. Target voltage ramps down to this value during graceful shutdown. Same as reference target, each bit represents one step of the reference DAC. LSB depends on the range.
C10B	04B	STA_SHTDN_STOP_THRESH_CH1[7:0]	7:0	
C20B	08B	STA_SHTDN_STOP_THRESH_CH2[7:0]	7:0	
C30B	0CB	STA_SHTDN_STOP_THRESH_CH3[7:0]	7:0	

2.6 Power Good Registers

This section defines the registers used to program the minimum and maximum voltage thresholds that define the “power good” range for channels 1-4.

Run time Address	Flash Address	Name	Bits	Description
C017	017	STA_PGOOD_THRES_UPPER_CH0[7:0]	0	ERROR_THRESH_MAX. Bit 8 of Power Good upper threshold.
C117	057	STA_PGOOD_THRES_UPPER_CH1[7:0]		
C217	097	STA_PGOOD_THRES_UPPER_CH2[7:0]	1	ERROR_THRESH_MIN. Bit 8 of Power Good upper threshold.
C317	0D7	STA_PGOOD_THRES_UPPER_CH3[7:0]	2	PFM2PWM_ERROR. Initial error value upon PFM-->PWM transition should correspond to comparator reference. Each bit represents one step in the encoded 9 bit error signal.
			7:3	U_OVS_FIRST_PULSE_MAX. After entering under voltage OVS mode, limit the first pulse to this duty ratio if u_ovs_first_pulse_limit is set high (each bit is 8 103 MHz clock cycles). Percentage of counter_restart_state/8 (50-90%).

Run time Address	Flash Address	Name	Bits	Description
C018	018	STA_PGOOD_THRES_MAX_LOWER_CH0[7:0]	7:0	Power Good Threshold Max. Each bit represents one step of the encoded 9 bit error signal.
C118	058	STA_PGOOD_THRES_MAX_LOWER_CH1[7:0]	7:0	
C218	098	STA_PGOOD_THRES_MAX_LOWER_CH2[7:0]	7:0	
C318	0D8	STA_PGOOD_THRES_MAX_LOWER_CH3[7:0]	7:0	
C019	019	STA_PGOOD_THRES_MIN_LOWER_CH0[7:0]	7:0	Power Good Threshold Min. Each bit represents one step of the encoded 9 bit error signal.
C119	059	STA_PGOOD_THRES_MIN_LOWER_CH1[7:0]	7:0	
C219	099	STA_PGOOD_THRES_MIN_LOWER_CH2[7:0]	7:0	
C319	0D9	STA_PGOOD_THRES_MIN_LOWER_CH3[7:0]	7:0	

2.6.1 Power Good Threshold Max Calculation

This section describes how to convert from the Power Good Threshold maximum value specified in GUI as a percentage of the target voltage to the value that should be written into the register.

The conversion equation used by the GUI is:

```
xr24['pgood_thresh_max_%d' % Channel] = (((int(round(inreg_below_voltage/0.0025)*4)))& 0x1FF) + 1
```

For example, if the Evaluation Board project file lists the following conditions:

- PowerArchitect version 5.02r2
- V_{OUT} 4 = 1V
- Resolution 2.5mV per step
- Power Good max threshold = 1%

Then the steps below can be used to calculate the equivalent register value.

Step 1 Calculate Rounded Value

Round[(((Power Good max threshold)/100*V_{target})) / (Resolution per step)]*4 = Round[((1/100*1)) / 0.0025]*4 = 16 => 0x10

Step 2 Truncate result to 9-bits

Mask result with 0x1FF to create a 9 bit value.

0x1FF AND 0x10 = 0x10

Step 3 Add 1 to the truncated value

0x10 + 1 = 0x11

The final register value is 0x11.

2.3.1 Power Good Threshold Min Calculation

This section describes how to convert from the Power Good Threshold minimum value specified in GUI as a percentage of the target voltage to the value that should be written into the register.

The conversion equation used by the GUI is:

```
xr24['pgood_thresh_min_%d' % Channel] = (((int(round(inreg_below_voltage/0.0025)*4))+1)& 0x1FF) - 1
```

For example, if the Evaluation Board project file lists the following conditions:

- PowerArchitect version 5.02r2
- V_{OUT} 4 = 1V
- Resolution 2.5mV per step
- Power Good max threshold = 1% below V_{TARGET}

Follow the steps below to calculate the equivalent register value.

Step 1 Calculate Rounded Value

Round[(((Power Good max threshold)/100*V_{target})) / (Resolution per step)]*4 = Round[((1/100*1)) / 0.0025]*4 = 16 = 0x10

Step 2 Calculate the 2's Complement

2's complement of 0x10 is 0x1F0.

Step 3 Truncate result to 9-bits

Mask result with 0x1FF to create a 9 bit value.

0x1FF AND 0x10 = 0x10

Step 4 Subtract 1 to the truncated value

0x1F0 - 1 = 0x1EF

The final register value is 0x1EF.

2.5 OVP Registers

This section provides the registers to program the static over voltage protection threshold per channel as well as the formulas to use to calculate the register value.

Runtime Address	Flash Address	Name	Bits	Description
C01A	01A	STA_OVP_THRES_CH0[6:0]	6:0	OVP Fault Threshold. Each bit represents one step of the original 7 bit error signal or VFDBK ADC quantization step.
C11A	05A	STA_OVP_THRES_CH1[6:0]	6:0	
C21A	09A	STA_OVP_THRES_CH2[6:0]	6:0	
C31A	0DA	STA_OVP_THRES_CH3[6:0]	6:0	

2.5.1 OVP Threshold Calculation

This section describes how to convert from the OVP threshold value specified in GUI to the value that should be written into the register.

The conversion equation used by the GUI is:

```
xr24['ovp_thresh_%d' % Channel] = ((int(round(inreg_below_voltage/0.0025)))& 0x7F)
```

For example, if the Evaluation Board project file lists the following conditions:

- PowerArchitect version 5.02r2
- V_{OUT} 4 = 1V
- Resolution 2.5mV per step
- OVP threshold = 10%

Follow the steps below to calculate the equivalent register value.

Step 1 Calculate Rounded Value

Round[(((OVP threshold)/100*V_{target})) / (Resolution per step)] = Round[((10/100*1)) / 0.0025] = 40 = 0x28

Step 2 Calculate the 2's Complement

2's complement of 0x28 is 0xD8.

Step 3 Truncate result to 7-bits

Mask result with 0x7F to create a 7 bit value.

0x7F AND 0xD8 = 0x58

The final register value is 0x58.

2.4 OCP Warning and Fault Registers

This section provides the over current protection registers and the formulas needed to calculate the values to program into the registers.

Runtime Address	Flash Address	Name	Bits	Description
C01B	01B	STA_OCPW_THRES_CH0[6:0]	6:0	OVC Warning Threshold. ADC_output = (160mV + (IFE_GAIN * (V_PGND - V_LX))) / 10mV if GAIN_8_ENABLE == 1'b1 then IFE_GAIN = 8, else IFE_GAIN = 4
C01C	01C	STA_OCPF_THRES_CH0[6:0]	6:0	
C11B	05B	STA_OCPW_THRES_CH1[6:0]	6:0	
C11C	05C	STA_OCPF_THRES_CH1[6:0]	6:0	
C21B	09B	STA_OCPW_THRES_CH2[6:0]	6:0	OVC Fault Threshold. ADC_output = (160mV + (IFE_GAIN * (V_PGND - V_LX))) / 10mV if GAIN_8_ENABLE == 1'b1 then IFE_GAIN = 8, else IFE_GAIN = 4
C21C	09C	STA_OCPF_THRES_CH2[6:0]	6:0	
C31B	0DB	STA_OCPW_THRES_CH3[6:0]	6:0	
C31C	0DC	STA_OCPF_THRES_CH3[6:0]	6:0	

2.4.1 OCP Calculation

The equation below can be used to calculate the OCP threshold value that should be programmed into the OCP registers. The load current is the lower range of the current ($I_{LVALLEY}$) plus the half the ripple current ($I_{PK\_PK\_RIPPLE}$). The warning threshold value that should be written into the register will be 85% of the over current threshold. Refer to the Application Note ANP-43 for a more in depth discussion of this calculation.

$V_{GL\_RTN} - V_{LX} = V_{IL} = (DEC(R_{VALUE})*0.01) / IFE\_GAIN) - 0.04$

$I_{LVALLEY} = V_{IL} / R_{DSON}$

$I_{PK\_PK\_RIPPLE} = (V_{IN} - V_{OUT})*V_{OUT} / V_{IN}*F_{SW}*L$

$I_{LOAD} = I_{LVALLEY} + (I_{PK\_PK\_RIPPLE} / 2)$

Warning Threshold value = $0.85 * I_{LOAD}$

A code sample taken from GUI software to calculate the over current limit is shown below.

```
FaultMult = 1.0

ChannelSwFreq = 1.0 / ((( self._Parameters['CounterRestartState'] + 1 ) / self._Parameters['FrequencyTier_%d' % Channel]) * 10e-9 )

Rdson = self._Parameters['Rdson_%d' % Channel]

CurrentMax = self._Parameters['Current_Max_%d' % Channel]

VinVolts = self._Parameters['InputVoltage_%d' % Channel]

VoutVolts = self._Parameters['OutputVoltage_%d' % Channel]

InductorH = self._Parameters['L_%d' % Channel]
```

```
Sampled_current_value_fault = 1.0 * Rdson * (# Average Current Limit Desired
  ( CurrentMax * FaultMult ) - (
 ( VinVolts - VoutVolts ) * ( VoutVolts / VinVolts ) * ( 1.0 / ChannelSwFreq ) / (2.0 * ChInd )
 ) + ( 60e-9 * VoutVolts / ChInd ))
Gain_8 = 1
# convert to ADC counts
Sampled_value_fault = int( (0.32 + ( 8.0 * Sampled_current_value_fault ) ) / 10e-3 )

#check if clipping and reduce gain
if (Sampled_value_fault > 0x7E):
    Gain_8 = 0
    Sampled_value_fault = int( (0.16 + ( 4.0 * Sampled_current_value_fault ) ) / 10e-3 )

#if its still clipping then set it to the max available, if 0x7F then OCP is disabled
if (Sampled_value_fault > 0x7E):
    xr24[‹ocpf_thresh_%d› % Channel]    = 0x7e
    ########### warn user
    logger.info(«Warning: OCP Fault handling threshold is being clipped for Channel %d « % (Channel+1))
else:
    xr24[‹ocpf_thresh_%d› % Channel]    = Sampled_value_fault
```

2.5 Ramp Continue Threshold Registers

This section defines the registers used to program the threshold for the start up power over which the device will limit the overshoot.

Runtime Address	Flash Address	Name	Bits	Description
C00C	00C	STA_RAMP_CONTINUE_THRESHOLD_CH0[6:0]	6:0	Ramp Continue Threshold. Set the threshold for the positive error value to reach in order to let the ramp continue in start-up, this is to prevent large overshoot in the beginning of the soft start. Each bit represents 1 step of the 9-bit encoded error. It can be determined by matlab program based on customer's preference in ramp-up speed.
C10C	04C	STA_RAMP_CONTINUE_THRESHOLD_CH1[6:0]	6:0	
C20C	08C	STA_RAMP_CONTINUE_THRESHOLD_CH2[6:0]	6:0	
C30C	0CC	STA_RAMP_CONTINUE_THRESHOLD_CH3[6:0]	6:0	

2.6 Predefined VIN Registers

This section defines the registers used to program the predefined external input voltage for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C01D	01D	STA_PREDEF_VIN_CH0[6:0]	6:0	Predefined VIN. To predefine external VIN value for the converter. Each bit represents one step of VIN resolution step. (200 mV LSB)
C11D	05D	STA_PREDEF_VIN_CH1[6:0]	6:0	
C21D	09D	STA_PREDEF_VIN_CH2[6:0]	6:0	
C31D	0DD	STA_PREDEF_VIN_CH3[6:0]	6:0	

2.7 Phase Positioning Registers

This section defines the registers used to program the 2-byte phase position for the PWM starting pulse for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C01F	01F	STA_SYNC_POSITION_UPPER_CH0[7:0]	7:0	Position for PWM start pulse[15:8]. Each bit represents one position in a fundamental period with 16 possible phase positions, for example, if a phase is operating at position d with a 4x switching frequency then this value should be set to:16'b1000_1000_1000_1000
C020	020	STA_SYNC_POSITION_LOWER_CH0[7:0]	7:0	
C11F	05F	STA_SYNC_POSITION_UPPER_CH1[7:0]	7:0	
C120	060	STA_SYNC_POSITION_LOWER_CH1[7:0]	7:0	
C21F	09F	STA_SYNC_POSITION_UPPER_CH2[7:0]	7:0	Position for PWM start pulse[7:0]. Each bit represents one position in a fundamental period with 16 possible phase positions, for example, if a phase is operating at position d with a 4x switching frequency then this value should be set to:16'b1000_1000_1000_1000
C220	0A0	STA_SYNC_POSITION_LOWER_CH2[7:0]	7:0	
C31F	0DF	STA_SYNC_POSITION_UPPER_CH3[7:0]	7:0	
C320	0E0	STA_SYNC_POSITION_LOWER_CH3[7:0]	7:0	

2.8 Current Sample Positioning Registers

This section defines the registers used to program the 2-byte phase position for the PWM starting pulse for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C021	021	STA_SYNC_CUR_POSITION_UPPER_CH0[7:0]	7:0	Position for current sampling pulse[15:8]. Each bit represents one position in a fundamental period with 16 possible sampling positions.
C022	022	STA_SYNC_CUR_POSITION_LOWER_CH0[7:0]	7:0	
C121	061	STA_SYNC_CUR_POSITION_UPPER_CH1[7:0]	7:0	
C122	062	STA_SYNC_CUR_POSITION_LOWER_CH1[7:0]	7:0	
C221	0A1	STA_SYNC_CUR_POSITION_UPPER_CH2[7:0]	7:0	Position for current sampling pulse[7:0]. Each bit represents one position in a fundamental period with 16 possible sampling positions.
C222	0A2	STA_SYNC_CUR_POSITION_LOWER_CH2[7:0]	7:0	
C321	0E1	STA_SYNC_CUR_POSITION_UPPER_CH3[7:0]	7:0	
C322	0E2	STA_SYNC_CUR_POSITION_LOWER_CH3[7:0]	7:0	

2.9 OVS Sample Positioning Registers

This section defines the registers used to program the 2-byte phase position for the PWM starting pulse for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C023	023	STA_SYNC_OVS_POSITION_UPPER_CH0[7:0]	7:0	Position for Current Sampling Pulse[15:8]. Each bit represents one position in a fundamental period with 16 possible sampling positions.
C024	024	STA_SYNC_OVS_POSITION_LOWER_CH0[7:0]	7:0	
C123	063	STA_SYNC_OVS_POSITION_UPPER_CH1[7:0]	7:0	
C124	064	STA_SYNC_OVS_POSITION_LOWER_CH1[7:0]	7:0	
C223	0A3	STA_SYNC_OVS_POSITION_UPPER_CH2[7:0]	7:0	Position for Current Sampling Pulse[7:0]. Each bit represents one position in a fundamental period with 16 possible sampling positions.
C224	0A4	STA_SYNC_OVS_POSITION_LOWER_CH2[7:0]	7:0	
C323	0E3	STA_SYNC_OVS_POSITION_UPPER_CH3[7:0]	7:0	
C324	0E4	STA_SYNC_OVS_POSITION_LOWER_CH3[7:0]	7:0	

2.10 PWM Configuration Registers

This section defines the registers used to program the PWM settings for channels 1-4.

2.10.1 PWM Max Duty Ratio Register

This section defines the registers used to program the PWM maximum duty cycle ratio for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C027	027	STA_PWM_MAX_DUTY_RATIO_CH0[7:0]	7:0	If calculated duty ratio is too close to 1, PWM duty will be always 1. Each bit represents one counter step with the 103MHz clock.
C127	067	STA_PWM_MAX_DUTY_RATIO_CH1[7:0]	7:0	
C227	0A7	STA_PWM_MAX_DUTY_RATIO_CH2[7:0]	7:0	
C327	0E7	STA_PWM_MAX_DUTY_RATIO_CH3[7:0]	7:0	

2.10.2 PWM Min Duty Ratio Register

This section defines the registers used to program the PWM minimum duty cycle ratio for channels 1-4.

Run time Address	Flash Address	Name	Bits	Description
C028	028	STA_PWM_MIN_DUTY_RATIO_CH0[7:0]	5:0	If calculated duty ratio is too close to 0, PWM duty will be always 0. Each bit represents one counter step with the 103MHz clock.
C128	068	STA_PWM_MIN_DUTY_RATIO_CH1[7:0]		
C228	0A8	STA_PWM_MIN_DUTY_RATIO_CH2[7:0]	7:6	Bits [9:8] of max_coarse_duty Each bit represents one counter step with the 103MHz clock.
C328	0E8	STA_PWM_MIN_DUTY_RATIO_CH3[7:0]		

2.10.3 PWM Configuration Register 1

Run time Address	Flash Address	Name	Bits	Description
C029 C129 C229 C329	029 069 0A8 0E8	STA_PWM_CONFIG1_CH0[7:0] STA_PWM_CONFIG1_CH1[7:0] STA_PWM_CONFIG1_CH2[7:0] STA_PWM_CONFIG1_CH3[7:0]	0	DISABLE_PWM_CHANNEL. Disable the PWM channel.
			3:1	DISABLE_CLOCK_GATING. Disable PWM/PFM/dead zone clock gating.
			6:4	STOP_WINDOW_ADVANCING_POINT. Defines for which duty values (LSB portion) the window should be advanced; default 4'd3. 3 LSB of duty ratio command (14 bits).
			7	ENABLE_WINDOW_DOUBLING. Doubles the width of the window signals controlling the reset point of the DPWM.

2.10.4 PWM Configuration Register 2

Run time Address	Flash Address	Name	Bits	Description
C02A C12A C22A C32A	02A 06A 0AA 0EA	STA_PWM_CONFIG2_CH0[3:0] STA_PWM_CONFIG2_CH1[3:0] STA_PWM_CONFIG2_CH2[3:0] STA_PWM_CONFIG2_CH3[3:0]	0	ENABLE_WINDOW_ADVANCING. Enables the window to be open early than it should in an ideal case.
			1	ENABLE_WINDOW_SLIDING. Enables DPWM window sliding.
			2	ENABLE_FORCED_SET_RESET. Enables the use of forced set/reset inputs for DPWM latches.
			3	ENABLE_EARLY_WINDOW_CLOSING. Enables early window closing.

2.10.5 Dead Time Control Registers

Runtime Address	Flash Address	Name	Bits	Description
C02B	02B	STA_PWM_DEADTIME_HS_UPPER_CH0[5:0]	5:0	Dead Time Control[13:0]. Dead-time value for turning on the high-side MOSFET. Each bit means one delay of the delay cell in DPWM or 600ps.
C02C	02C	STA_PWM_DEADTIME_HS_LOWER_CH0[7:0]	7:0	
C02D	02D	STA_PWM_DEADTIME_LS_UPPER_CH0[5:0]	5:0	
C02E	02E	STA_PWM_DEADTIME_LS_LOWER_CH0[7:0]	7:0	
C12B	06B	STA_PWM_DEADTIME_HS_UPPER_CH1[5:0]	5:0	
C12C	06C	STA_PWM_DEADTIME_HS_LOWER_CH1[7:0]	7:0	
C12D	06D	STA_PWM_DEADTIME_LS_UPPER_CH1[5:0]	5:0	
C12E	06E	STA_PWM_DEADTIME_LS_LOWER_CH1[7:0]	7:0	
C22B	0AB	STA_PWM_DEADTIME_HS_UPPER_CH2[5:0]	5:0	
C22C	0AC	STA_PWM_DEADTIME_HS_LOWER_CH2[7:0]	7:0	
C22D	0AD	STA_PWM_DEADTIME_LS_UPPER_CH2[5:0]	5:0	
C22E	0AE	STA_PWM_DEADTIME_LS_LOWER_CH2[7:0]	7:0	
C32B	0EB	STA_PWM_DEADTIME_HS_UPPER_CH3[5:0]	5:0	
C32C	0EC	STA_PWM_DEADTIME_HS_LOWER_CH3[7:0]	7:0	
C32D	0ED	STA_PWM_DEADTIME_LS_UPPER_CH3[5:0]	5:0	
C32E	0EE	STA_PWM_DEADTIME_LS_LOWER_CH3[7:0]	7:0	

2.11 Saturation Limit Register

This section describes the registers that are used to configure the PID saturation limit.

Runtime Address	Flash Address	Name	Bits	Description
C02F	02F	STA_SAT_LIM_DUTY_FB_CH0[7:0]	7:0	Sets the absolute limit for saturation block in PID calculation, normally a little higher than counter_restart_state_0[9:1]. Each bit represents 4 counts of the counter running off 103MHz frequency.
C12F	06F	STA_SAT_LIM_DUTY_FB_CH1[7:0]	7:0	
C22F	0AF	STA_SAT_LIM_DUTY_FB_CH2[7:0]	7:0	
C32F	0EF	STA_SAT_LIM_DUTY_FB_CH3[7:0]	7:0	

2.12 Target Voltage Setting Register

This section describes the registers that are used to configure the DAC target voltage.

Runtime Address	Flash Address	Name	Bits	Description
C032	032	DYN_VREF_TARG_CH0[7:0]	7:0	Sets target voltage in the reference DAC resolution. Each bit means 12.5mV (reference DAC resolution) when prescaler is set to 2'b00; 25mV with prescaler 2'b01 and 50mV with prescaler=2'b10
C132	072	DYN_VREF_TARG_CH1[7:0]	7:0	
C232	0B2	DYN_VREF_TARG_CH2[7:0]	7:0	
C332	0F2	DYN_VREF_TARG_CH3[7:0]	7:0	

2.13 Ramp Up/Down Setting Registers

This section describes the DAC ramp up/down settings and the formulas required to calculate the values to program into the registers.

Runtime Address	Flash Address	Name	Bits	Description
C033	033	DYN_UP_SLOPE_CH1[7:0]	7:0	Ramp Up Rate. Defines the ramp-up speed in terms of the number of switching cycles between increments of the reference DAC steps. Each bit represents one switching cycle between the reference DAC steps.
C133	073	DYN_UP_SLOPE_CH2[7:0]	7:0	
C233	0B3	DYN_UP_SLOPE_CH3[7:0]	7:0	
C333	0F3	DYN_UP_SLOPE_CH4[7:0]	7:0	
C034	034	DYN_DOWN_SLOPE_CH1[7:0]	7:0	Ramp Down Rate. Defines the ramp-down speed in terms of the number of switching cycles between increments of the reference DAC steps. Each bit represents one switching cycle between the reference DAC steps.
C134	074	DYN_DOWN_SLOPE_CH2[7:0]	7:0	
C234	0B4	DYN_DOWN_SLOPE_CH3[7:0]	7:0	
C334	0F4	DYN_DOWN_SLOPE_CH4[7:0]	7:0	

2.13.1 Ramp Up/Down Calculations

The formula below can be used to calculate the values for the ramp up/down registers.

Register Value (decimal) = (Ramp rate (ms/V) * f_{sw} kHz * V_{TARGET}) / (Number of DAC steps)

The value for the slope is the number of switching cycles between DAC steps. Channels with longer ramp times will have a higher DAC setting and a lower switching frequency.

The following example describes how to calculate the ramp up time. The same procedure can be used to calculate the ramp down time.

Given:

- Ramp rate set in GUI = 5.020
- f_{sw} = 494kHz
- V_{TARGET} = 3.3V
- 66 DAC steps

The register value can be calculated using the formula below.

Register Value (decimal) = (5.020 ms/V * 494kHz * 3.3V) / 66 = 123 or 0x7B

To then determine the maximum ramp time, use the formula below:

(DAC steps) * (Max register setting) / f_{sw} = 66 * 255 /494kHz = ~34msec

which is 10.32msec/V, which corresponds to the maximum GUI value of 255.

2.14 PID Configuration Registers

This section describes the registers that are used to configure the PID settings.

2.14.1 PID Coefficients Registers

This section describes the registers that are used to program the A-E PID coefficients for channels 1-4.

Runtime Address	Flash Address	Name	Bits	Description
C035	035	DYN_PID_A_UPPER_CH0	14:8	Channel 0 PID coefficient A[14:0].
C036	036	DYN_PID_A_LOWER_CH0	7:0	
C037	037	DYN_PID_B_UPPER_CH0	14:8	Channel 0 PID coefficient B[14:0].
C038	038	DYN_PID_B_LOWER_CH0	7:0	
C039	039	DYN_PID_C_UPPER_CH0	14:8	Channel 0 PID coefficient C[14:0].
C03A	03A	DYN_PID_C_LOWER_CH0	7:0	
C03B	03B	DYN_PID_D_CH0	6:0	Channel 0 PID coefficient D[6:0].
C03C	03C	DYN_PID_E_CH0	6:0	Channel 0 PID coefficient E[6:0].
C135	075	DYN_PID_A_UPPER_CH1	14:8	Channel 1 PID coefficient A[14:0].
C136	076	DYN_PID_A_LOWER_CH1	7:0	
C137	077	DYN_PID_B_UPPER_CH1	14:8	Channel 1 PID coefficient B[14:0].
C138	078	DYN_PID_B_LOWER_CH1	7:0	
C139	079	DYN_PID_C_UPPER_CH1	14:8	Channel 1 PID coefficient C[14:0].
C13A	07A	DYN_PID_C_LOWER_CH1	7:0	
C13B	07B	DYN_PID_D_CH1	6:0	Channel 1 PID coefficient D[6:0].
C13C	07C	DYN_PID_E_CH1	6:0	Channel 1 PID coefficient E[6:0].
C235	0B5	DYN_PID_A_UPPER_CH2	14:8	Channel 2 PID coefficient A[14:0].
C236	0B6	DYN_PID_A_LOWER_CH2	7:0	
C237	0B7	DYN_PID_B_UPPER_CH2	14:8	Channel 2 PID coefficient B[14:0].
C238	0B8	DYN_PID_B_LOWER_CH2	7:0	
C239	0B9	DYN_PID_C_UPPER_CH2	14:8	Channel 2 PID coefficient C[14:0].
C23A	0BA	DYN_PID_C_LOWER_CH2	7:0	
C23B	0BB	DYN_PID_D_CH2	6:0	Channel 2 PID coefficient D[6:0].
C23C	0BC	DYN_PID_E_CH2	6:0	Channel 2 PID coefficient E[6:0].
C335	0F5	DYN_PID_A_UPPER_CH3	14:8	Channel 3 PID coefficient A[14:0].
C336	0F6	DYN_PID_A_LOWER_CH3	7:0	
C337	0F7	DYN_PID_B_UPPER_CH3	14:8	Channel 3 PID coefficient B[14:0].
C338	0F8	DYN_PID_B_LOWER_CH3	7:0	
C339	0F9	DYN_PID_C_UPPER_CH3	14:8	Channel 3 PID coefficient C[14:0].
C33A	0FA	DYN_PID_C_LOWER_CH3	7:0	
C33B	0FB	DYN_PID_D_CH3	6:0	Channel 3 PID coefficient D[6:0].
C33C	0FC	DYN_PID_E_CH3	6:0	Channel 3 PID coefficient E[6:0].

2.14.2 PID Gain, Scaler, PFM and OVS Enable Registers

This section describes the registers that are used to enable PFM and OVS modes as well as set the PID gain and the DAC voltage divider value.

Run time Address	Flash Address	Name	Bits	Description
C03D C13D C23D C33D	03D 07D 0BD 0FD	DYN_PRESCALER_CH0[7:0] DYN_PRESCALER_CH1[7:0] DYN_PRESCALER_CH2[7:0] DYN_PRESCALER_CH3[7:0]	2:0	PID Gain Shifter. The selected value represents a power of two multiplier. For example, 011 would set the PID gain to 8 times the original gain.
			3	Enable Oversampling. Enables oversampling/overswitching in PWM mode only.
			5:4	DAC Prescaler and Voltage Divider. 00 Output set to original gain 01 Output divided by 2 10 Output divided by 4 11 Reserved
			6	Enable PFM. When set, this bit enables PFM operation.
			7	Enable OVS. When set, this bit enable OVS operation only during the PFM to PWM transition.

2.14.3 Zero Error Bin Shift, PID Ramp Gain Registers

These registers can be used to verify (read) the voltage set point after a dynamic change. However, changing (writing) the values must be done using the standard I²C commands 0x20 through 0x23 as explained in ANP-38.

Run time Address	Flash Address	Name	Bits	Description
C03E C13E C23E C33E	03E 07E 0BE 0FE	DYN_ZERO_ERROR_BIN_SHIFT_CH0[6:0] DYN_ZERO_ERROR_BIN_SHIFT_CH1[6:0] DYN_ZERO_ERROR_BIN_SHIFT_CH2[6:0] DYN_ZERO_ERROR_BIN_SHIFT_CH3[6:0]	2:0	ZERO_ERROR_BIN_SHIFT. Fine adjustment with 2.5mV/5mV/10mV steps in PWM mode depending on the scaler.
			3	ENABLE_PREBIAS_CHK. Enables the prebias prevention option where the PID won't start until reference ramp is above the pre-bias voltage at output.
			6:4	PID_GAIN_RAMP. PID gain shifter during ramp up and ramp down; value represents powers of 2. For example, 011 means 8 times original gain.

2.15 Non-linear Encoding, Temperature Sampling, Median Filter Bypass Register

This section describes the registers that are used to configure a variety of features such as temperature sampling, bypass filter settings, and non-linear encoding.

Run time Address	Flash Address	Name	Bits	Description
C400	100	STA_ERR_NONLINEAR_ENCODING[7:0]	0	NONLINEAR . Enables the nonlinear error encoding scheme.
			1	RESERVED
			2	TEMPENABLEHOLD. Enables temperature sampled at switching fundamental frequency if any channel is in PWM mode. When disabled, only on-demand temperature sampling is available.
			3	RESERVED
			4	BYPASS_CURRENT_FILTER. Enables bypass median filter for current sense measurements.
			5	BYPASS_VIN_FILTER. Enables bypass median filter for VIN measurements.
			6	BYPASS_TEMP_FILTER. Enables bypass median filter for temperature measurements.
			7	BYPASS_VOUT_FILTER. Enables bypass median filter for VOUT measurements.

2.16 Fault Following Registers

This section describes the registers that are used to configure the fault following bits per channel.

Run time Address	Flash Address	Name	Bits	Description
C401	101	STA_FAULT_FOLLOWS_UPPER[3:0]	3:0	Fault Following Configuration: | Following channel | Leader | Set follows bit Channel 1 | Channel 2 | 0 | Channel 3 | 1 | Channel 4 | 2 Channel 2 | Channel 1 | 3 | Channel 3 | 4 | Channel 4 | 5 Channel 3 | Channel 1 | 6 | Channel 2 | 7 | Channel 4 | 8 Channel 4 | Channel 1 | 9 | Channel 2 | 10 | Channel 3 | 11
C402	102	STA_FAULT_FOLLOWS_UPPER[7:0]	7:0	

2.17 Over Temperature Protection (OTP) Warning, Fault Thresholds and Thermal Restart Registers

This section describes the registers that are used to configure the temperature related features.

Runtime Address	Flash Address	Name	Bits	Description
C403	103	STA_OTPW_THRES[6:0]	6:0	Over temperature warning threshold. 5 Kelvin per LSB

Runtime Address	Flash Address	Name	Bits	Description
C404	104	STA_OTPF_THRES[6:0]	6:0	Over temperature fault threshold. 5 Kelvin per LSB
C405	105	STA_OVT_THERMAL_RESTART[6:0]	6:0	Thermal restart threshold. After this threshold is passed, a soft reset will be generated. 5 Kelvin per LSB.

2.18 Under Voltage Lockout (UVLO) Warning, Fault Thresholds Registers

This section describes the registers that are used to configure the UVLO features.

Runtime Address	Flash Address	Name	Bits	Description
C406	106	STA_UVLOW_THRES[6:0]	6:0	UVLO warning threshold. 200mV LSB.
C407	107	STA_UVLOF_THRES[6:0]	6:0	UVLO fault threshold. 200mV LSB.

2.19 External Driver Mode Registers

This section describes the registers that are used to enable the external drivers per channel.

Runtime Address	Flash Address	Name	Bits	Description
C408	108	STA_EXTERNAL_DRIVER_MODE[3:0]	3:0	Enables external drivers on per channel basis. Bit 0 Channel 1 Bit 1 Channel 2 Bit 2 Channel 3 Bit 3 Channel 4

2.20 VIN Selector Registers

This section describes the registers that are used to configure the input voltage selection.

Run time Address	Flash Address	Name	Bits	Description
C409	109	STA_VIN_SELECTOR[5:0]	3:0	INPUT_VOLTAGE_SEL. Selects between the measured input voltage and the specified value for the four channels in case of a second Vin source. For each bit, '1' selects the predefined Vin, '0' selects the measured Vin. Bit 0 Channel 1 Bit 1 Channel 2 Bit 2 Channel 3 Bit 3 Channel 4
			5:4	FILTER_LENGTH. Bit length of the comparator digital filter, which is the number of cycles in terms of delay. Each bit corresponds to a delay of 10nS.

2.21 Fundamental Frequency and Frequency Multipliers Registers

This section describes the registers that are used to configure the fundamental and switching frequency settings.

Runtime Address	Flash Address	Name	Bits	Description
C40A	10A	STA_COUNTER_RESTART_STATE_UPPER[1:0]	1:0	Fundamental frequency[9:0]. Each bit represents one counter step with the 103MHz system clock.
C40B	10B	STA_COUNTER_RESTART_STATE_LOWER[7:0]	7:0	
C40C	10C	STA_FREQUENCY_TIER[7:0]	7:0	Switching frequency - 2 bits per channel. 2'b00 selects the fundamental frequency; 2'b01 selects 2X frequency; 2'b1x 4 selects X frequency. Bits [1:0] Channel 1 Bits [2:3] Channel 2 Bits [4:5] Channel 3 Bits [6:7] Channel 4

2.22 VIN, Temperature Sample Positioning Registers

This section describes the registers that are used to configure the phase positions for the input voltage and temperature measurements.

Runtime Address	Flash Address	Name	Bits	Description
C40D	10D	STA_SYNC_VIN_POSITION_UPPER[7:0]	7:0	Specifies the phase position for Vin measurements[15:0]. Each bit represents one Vin sampling position in a fundamental period with 16 possible positions; for example, 16'b1000_1000_1000_1000 means to sample VIN four times at the phase positions that are ones in a fundamental cycle.
C40E	10E	STA_SYNC_VIN_POSITION_LOWER[7:0]	7:0	

Runtime Address	Flash Address	Name	Bits	Description
C40F	10F	STA_SYNC_TEMP_POSITION_ UPPER[7:0]	7:0	Specifies the phase position for temperature measurements[15:8]. Each bit represents one temperature sampling position in a fundamental period with 16 possible positions; for example, 16'b1000_1000_1000_1000 means to sample four times at the phase positions that are ones in a fundamental cycle.
C410	110	STA_SYNC_TEMP_POSITION_ LOWER[7:0]	7:0	

2.23 ADC Configuration Registers

This section describes the registers that are used to configure the ADC.

2.23.1 Feedback ADC Sampling Time Registers

This section describes the registers that are used to configure the ADC sampling feedback settings.

Runtime Address	Flash Address	Name	Bits	Description
C411	111	STA_SYNC_ADC_PULSE_LEAD[5:0]	7:0	Specifies the time between voltage ADC sampling point to the beginning of next cycle. Each bit represents one counter step with the 103MHz clock.
C412	112	STA_SYNC_ADC_LATCH_LEAD[5:0]	7:0	Specifies the time between voltage ADC latching point to the beginning of next cycle. Each bit represents one counter step with the 103MHz clock.

2.23.2 Auxiliary ADC Sampling Time Registers

This section describes the registers that are used to configure the auxiliary ADC sampling times.

Runtime Address	Flash Address	Name	Bits	Description
C413	113	STA_SYNC_AUX_PULSE_LEAD[5:0]	5:0	Specifies the time between auxiliary ADC sampling point to the beginning of next cycle. Each bit represents one counter step with the 103MHz clock.
C414	114	STA_SYNC_AUX_LATCH_LEAD[5:0]	5:0	Specifies the time between auxiliary ADC latching point to the beginning of next cycle. Each bit represents one counter step with the 103MHz clock.

2.23.3 Force Duty Ratio Registers

This section describes the registers that are used to configure the forced duty cycle ratio if enabled in the "Bypass Sigma Delta, Force Duty Mode Registers". These registers should only be used during test.

Runtime Address	Flash Address	Name	Bits	Description
C415	115	STA_TEST_FORCED_DUTY_UPPER[5:0]	5:0	Forced duty ratio[13:0]
C416	116	STA_TEST_FORCED_DUTY_LOWER[7:0]	7:0	14 bit duty ratio command. Each bit represent one delay in VCO or 600ps, the 10 MSB has to be less than counter_ restart_state@C40A

2.23.4 Bypass Sigma Delta, Force Duty Mode Registers

This section describes the registers that are used to enable forced duty cycle mode and to disable sigma delta mode.

Run time Address	Flash Address	Name	Bits	Description
C417	117	STA_SIGDEL_BYPASS[7:0]	3:0	BYPASS_SIGDEL. Disables the sigma delta.
			7:4	FORCED_DUTY_MODE. Enables the forced duty ratio mode. Bit 4 Channel 1 Bit 5 Channel 2 Bit 6 Channel 3 Bit 7 Channel 4

2.23.5 Auxiliary ADC VOUT Sampling Time Registers

This section describes the registers that are used to configure the phase position for the ADC output voltage.

Runtime Address	Flash Address	Name	Bits	Description
C418	118	STA_SYNC_VOUT_POSITION_ UPPER[7:0]	7:0	Specifies the phase position for Vout measurements in with auxiliary ADC[15:0] Each bit represents one on demand VOUT sampling position in a fundamental period with 16 possible positions; for example, 16'b1000_1000_1000_1000 means to sample four times at the phase positions that are ones in a fundamental cycle.
C419	119	STA_SYNC_VOUT_POSITION_ LOWER[7:0]	7:0	

2.23.6 Auxiliary ADC Sampling Time Registers

This section describes the registers that are used to configure the sampling settings for the auxiliary ADC.

Runtime Address	Flash Address	Name	Bits	Description
C41A	11A	STA_AFE_CH_SEL_START[5:0]	5:0	Specifies the number of clock cycles before the start of the next sampling period when isense_ch_sel and aux_vout_sel go high. Each bit represents one counter step with the 103MHz clock.
C41B	11B	STA_AFE_CH_SEL_FINISH[5:0]	5:0	Specifies the number of clock cycles after the start of a sampling period when isense_ch_sel and aux_vout_sel go low. Each bit represents one counter step with the 103MHz clock.
C41C	11C	STA_AUX_ADC_SEL_START[5:0]	5:0	Specifies the number of clock cycles before the start of the next sampling period when aux_adc_sel go high. Each bit represents one counter step with the 103MHz clock.
C41D	11D	STA_AUX_ADC_SEL_FINISH[5:0]	5:0	Specifies the number of clock cycles after the start of a sampling period when aux_adc_sel go low. Each bit represents one counter step with the 103MHz clock.

2.23.7 Auxiliary ADC VOUT Sampling Time Register

This section describes the registers that are used to configure the sampling settings for the auxiliary ADC output voltage.

Runtime Address	Flash Address	Name	Bits	Description
C41E	11E	STA_VFDBK_CH_SEL_START[5:0]	5:0	Specifies the number of clock cycles before the start of a sampling period when vfdbk_ch_sel will change. Each bit represents one counter step with the 103MHz clock.

2.24 General Control 1 Registers

This section describes the registers that are used to configure a variety of control settings.

Runtime Address	Flash Address	Name	Bits	Description
D001	141	VCO_FREQUENCY_CTRL[3:0]	3:0	VCO Pull Range Clamp Limit.
D002	142	DPWM_SELECT_CLOCK_PHASE[1:0]	1:0	Clock Phase Selection.
D003	143	DPWM_WINDOW_SELECT[1:0]	1:0	Jitter Window Timing Selection.
D004	144	ICP_SELECT[5:0]	5:0	Charge Pump Current Selection.
D005	145	JITTERFILTER_DISABLE	0	Jitter Filter Disable.
D006	146	AUVLO_THRESHOLD[7:0]	7:0	Fixed to 100mV LSB in XRP7724
D007	147	LDOB_LEVEL_SELECT[1:0]	1:0	00 3.3V 01 3.15V 10 3.15V 11 3.0V
D008	148	RESERVED		
D009	149	ADC_AFE_DIV_CON[3:0]	3:0	Resistor divider enable signal for YFLASH charge pump test.

2.25 PFM Target Registers

This section describes the registers that are used to configure the PFM target signal settings.

Runtime Address	Flash Address	Name	Bits	Description
D00A	14A	PFM_VTAR_ABOVE_SEL_CH0[3:0]	3:0	PFM Comparator Above VTAR Selection Signal. 0 to 7 0% to 7% above VTAR 8 to F -1% to -8% below VTAR
D00B	14B	PFM_VTAR_ABOVE_SEL_CH1[3:0]	3:0	
D00C	14C	PFM_VTAR_ABOVE_SEL_CH2[3:0]	3:0	
D00D	14D	PFM_VTAR_ABOVE_SEL_CH3[3:0]	3:0	
D00E	14E	PFM_VTAR_BELOW_SEL_CH0[3:0]	3:0	PFM Comparator Below VTAR Selection Signal. 0 to 7 0% to 7% above VTAR 8 to F -1 to -8% below VTAR
D00F	14F	PFM_VTAR_BELOW_SEL_CH1[3:0]	3:0	
D010	150	PFM_VTAR_BELOW_SEL_CH2[3:0]	3:0	
D011	151	PFM_VTAR_BELOW_SEL_CH3[3:0]	3:0	

2.26 General Control 2 Registers

This section describes the registers that are used to configure a variety of control settings.

Runtime Address	Flash Address	Name	Bits	Description
D012	152	RESERVED		
D013	153	RESERVED		
D014	154	RESERVED		
D015	155	DRIVER_EXNOV_EN_CH[3:0]	3:0	If set to “1” programmable dead time is used. If set to “0” the internal driver dead time is applied. Bit 0 Channel 1 Bit 1 Channel 2 Bit 2 Channel 3 Bit 3 Channel 4

Runtime Address	Flash Address	Name	Bits	Description
D016	156	ISENSE_IFE_GAIN8_ENABLE[3:0]	3:0	If “1” set to the IFE_GAIN of 8 is selected. If set to ‘0’, the IFE_GAIN of 4 is selected. Bit 0 Channel 1 Bit 1 Channel 2 Bit 2 Channel 3 Bit 3 Channel 4
D017	157	RESERVED		
D018	158	V5EXT_SWITCH_CONTROL[3:0]	3:0	Bit 0 If set to “0” prevents LDO5 from shutting down even after 5V switchover Bit 1 If set to “1”, forces 5V switchover pass device off and forces LDO5 on Bit 2 If set to “0”, it resets 5V switchover circuit, shuts off 5V switchover pass device and forces LDO5 on
D019	159	RESERVED		
D01A	15A	RESERVED		

2.27 Clock Control Registers

This section describes the registers that are used to configure the PLL, VCO and OSC clocks.

2.27.1 Clock Control Register 0

This section describes the registers that are used to configure the

Run time Address	Flash Address	Name	Bits	Description
D01B	15B	CGC_WAIT[5:0]	1:0	PLL_LOCK_WAIT. Specifies how long to wait after the PLL has been enabled before checking the lock signal and allowing a transition to another mode. Nominal value is 400µs.
			3:2	VCO_TURN_ON_WAIT. Specifies how long to wait to switch the output clock to the VCO after it has been turned on. Nominal value is 400ns.
			5:4	OSC_TURN_ON_WAIT. Specifies how long to wait to switch the output clock to the oscillator after it has been turned on. Nominal value is 100ns.

2.27.2 Clock Control Register 1

Contact Exar Technical Support before making changes to this register/

Run time Address	Flash Address	Name	Bits	Description
D01C	15C	CGC_MODE_1[7:0]	0	EXTCLK_OUT_ENABLED.
			1	EXTCLK_IN_ENABLED.
			2	EXTCLK_OUT_ENABLE_OVERRIDE_STANDBY.
			3	EXTCLK_OUT_ENABLE_OVERRIDE_OSCILLATOR.
			4	FORCE_VCO_PLL_MODE.
			5	FORCE_VCO_MODE.
			6	FORCE_CLOCK_MODE.
			7	PLL_IGNORE_LOCK.

2.27.3 Clock Control Register 2

This register is used to configure the standby and wakeup modes for the clocks.

Run time Address	Flash Address	Name	Bits	Description
D01D	15D	CGC_MODE_2[7:0]	0	STANDBY_ENABLE. Setting this bit will force the XRP7724 to enter standby mode..
			1	TEST_MODE. If enabled the XRP7724 will not enter standby mode until this bit is set low again.
			2	RESERVED
			3	DISABLE_AUVLO_WAKEUP. If enabled the XRP7724 clock will not be woken from the AUVLO setting in the GUI.
			4	DISABLE_LDOA_OVC_WAKEUP. If enabled the XRP7724 clock will not be woken if LDO5 current limit is reached.
			5	DISABLE_LDOB_OVC_WAKEUP. If enabled the XRP7724 clock will not be woken if LDO3_3 current limit is reached.
			6	Reserved.
			7	DISABLE_V5EXT_WAKEUP. If enabled the XRP7724 clock will not be woken by the V5EXT signal.

2.27.4 External Clock Mode Registers

Run time Address	Flash Address	Name	Bits	Description
D01E	15E	EXT_CLOCK_MODE[6:0]	0	DIVIDE_RATIO_IN. Sets the clock divider ratio for the system input clock. 1 Divide by 4 0 Divide by 8
			1	DIVIDE_RATIO_OUT. Sets the clock divider ratio for the system output clock. 1 Divide by 4 0 Divide by 8
			3:2	RANGE. Sets the valid range for the input clock detection. 00 25% 01 20% 10 15% 11 10%
			5:4	SET_ENABLE_HF. Enables high frequency operation for the PSIOs and GPIOs. Bit 4 sets PSIOs and Bit 5 sets GPIOs. 1 High frequency mode 0 Standard frequency mode
			6	EXT_CLK_IN_VALID_OVERRIDE. If enabled the current external clock input will be considered present and in the valid range. This bit should not be set during normal operation.

2.28 Boost Feedback Control

This register is used to enable and fine-tune the boost control feedback feature. All fields in this register require bit 3 BOOST_FDBK_EN to be set.

Run time Address	Flash Address	Name	Bits	Description
D01F	15F	BFB_V_SEL[6:0]	2:0	BFB_V_SEL. Customer programmable field to adjust the boost feedback from 9-16V. Each bit represents 1V.
			3	BOOST_FDBK_EN. Enables the boost feedback feature.
			5:4	BOOST_FDBK_CH. Specifies which channel is connected to the boost charge pump: 00 Channel 1 01 Channel 2 0 Channel 3 11 Channel 4
			6	REDUCE_BFB_PFM_PULSES. If enabled the duty ratio of the boost feedback pulses will be divided again by 2 before being sent to the DPWM. This can feature can ensure that the positive average current is never sent for boost feedback pulses.

2.29 Control Registers

These registers are used to control the power systems for the XRP7724 device.

Runtime Address	Flash Address	Name	Bits	Description
D020	160	RESERVED		
D021	161	ENABLE_SWITCHING_PERIOD_COUNT[5:0]	5:0	PFM Frequency Measurement Enable. 1xxxxx Enable frequency measurement in PFM mode All others reserved.
D022	162	RESERVED		
D023	163	V5EXT_THRESHOLD_HIGH[3:0]	3:0	External 5V Upper Threshold. 0001 4.7V 0010 4.75V 0100 4.80V 1000 4.85V
D024	164	V5EXT_THRESHOLD_LOW[3:0]	3:0	External 5V Lower Threshold: 0001 4.55V 0010 4.60V 0100 4.65V 1000 4.70V
D025	165	POWERUP_LDOB [5:0]	5:0	LDO Enable. xxxxx0 Enable LDO_3.3 All others reserved.
D026	166	RESERVED		

2.30 I/O Configuration Registers

This section defines the registers used to control the device I/O.

2.30.1 I/O Clock Wake Up Control

These registers are used to enable/disable the GPIO and PSIO from waking the system clock.

Run time Address	Flash Address	Name	Bits	Description
D027	167	DISABLE_GPIO_PSIO_WAKEUP[4:0]	1:0	DISABLE_GPIO_WAKEUP. Prevents a GPIO from waking up the clock. Bit 0 GPIO0 Bit 1 GPIO1
			4:2	DISABLE_PSIO_WAKEUP. Prevents a PSIO from waking up the clock. Bit 2 PSIO0 Bit 3 PSIO1 Bit 4 PSIO2

2.30.2 I/O Control Registers

These registers are used to configure the GPIO and PSIO.

Runtime Address	Flash Address	Name	Bits	Description
D302	168	SET_GPIO0_CFG[7:0]	7:0	Set GPIO0 Configuration. 0x60 PLL clock input 0x61 General input 0x00 All others
D303	169	SET_GPIO1_CFG[7:0]	7:0	Set GPIO1 Configuration. 0x54 PLL clock input 0x61 General input 0x00 All others
D304	16A	SET_PSIO0_CFG[7:0]	7:0	Set PSIO0 Configuration. 0x61 General input 0x00 All others
D305	16B	SET_PSIO1_CFG[7:0]	7:0	Set PSIO1 Configuration. 0x61 General input 0x00 All others
D306	16C	SET_PSIO2_CFG[7:0]	7:0	Set PSIO2 Configuration. 0x61 General input 0x00 All others
D307	16D	RESERVED		

Runtime Address	Flash Address	Name	Bits	Description
D308	16E	GPIO_PSIO_POLARITY[7:0]	7:0	I/O polarity. Bitwise setting of the I/O polarity. Setting a bit to "1" corresponds to inverted polarity. Bit 0 GPIO 0 Bit 1 GPIO 1 Bit 2 PSIO 0 Bit 3 PSIO 1 Bit 4 PSIO 2 All other values are reserved.

2.31 Special Function Registers

These registers are used to read and mask the XRP7724 interrupts as well as access other special functions. Note that not all special function registers are accessible though the Flash. Refer to Application Note ANP-38 for detailed information about programming the Flash.

Run-Time-Address	Flash Address	Name	Bits	Description	Type
FFA0		RESERVED			
FFA1		INT_CTLLR[6:0]	0	OVP UVLO OTP INTERRUPT	R
			1	OCP INTERRUPT	
			2	LDO INTERRUPT	
			3	INREGULATION INTERRUPT	
			4	GENERAL INTERRUPT	
			5	TIMER INTERRUPT	
			6	GPIO_PSIO INTERRUPT	
			7	RESERVED	
FFA2	173	INT_CTLLR_MASK[7:0]	0	OVP UVLO OTP INTERRUPT MASK	R/W
			1	OCP INTERRUPT MASK	
			2	LDO INTERRUPT MASK	
			3	INREGULATION INTERRUPT MASK	
			4	GENERAL INTERRUPT MASK	
			5	TIMER INTERRUPT MASK	
			6	GPIO INTERRUPT MASK	
			7	PSIO INTERRUPT MASK	
FFA3		OVP_UVLO_OTP_INT[7:0]	0	OVP FAULT Channel 1	R/W
			1	OVP FAULT Channel 2	
			2	OVP FAULT Channel 3	
			3	OVP FAULT Channel 4	
			4	UVLO WARNING	
			5	UVLO FAULT	
			6	OTP WARNING	
			7	OTP FAULT	

Run-Time-Address	Flash Address	Name	Bits	Description	Type
FFA4	174	OVP_UVLO_OTP_MASK[7:0]	0	OVP FAULT MASK Channel 1	R/W
			1	OVP FAULT MASK Channel 2	
			2	OVP FAULT MASK Channel 3	
			3	OVP FAULT MASK Channel 4	
			4	UVLO WARNING MASK	
			5	UVLO FAULT MASK	
			6	OTP WARNING MASK	
			7	OTP FAULT MASK	
FFA5		OCP_INT[7:0]	0	OCP FAULT Channel 1	R/W
			1	OCP FAULT Channel 2	
			2	OCP FAULT Channel 3	
			3	OCP FAULT Channel 4	
			4	OCP WARNING Channel 1	
			5	OCP WARNING Channel 2	
			6	OCP WARNING Channel 3	
			7	OCP WARNING Channel 4	
FFA6	175	OCP_MASK[7:0]	0	OCP FAULT MASK Channel 1	R/W
			1	OCP FAULT MASK Channel 2	
			2	OCP FAULT MASK Channel 3	
			3	OCP FAULT MASK Channel 4	
			4	OCP WARNING MASK Channel 1	
			5	OCP WARNING MASK Channel 2	
			6	OCP WARNING MASK Channel 3	
			7	OCP WARNING MASK Channel 4	
FFA7		LDO_INT[7:0]	0	LDO3.3OK RISE	R/W
			1	LDO3.3OK FALL	
			2	LDO3.3OVC RISE	
			3	LDO3.3OVC FALL	
			4	LDO5OVC RISE	
			5	LDO5OVC FALL	
			6	V5EXT CONTROL RISE	
			7	V5EXT CONTROL FALL	
FFA8		RESERVED			
FFA9	176	LDO_MASK[7:0]	0	LDO3.3OK RISE MASK	R/W
			1	LDO3.3OK FALL MASK	
			2	LDO3.3OVC RISE MASK	
			3	LDO3.3OVC FALL MASK	
			4	LDO5OVC RISE MASK	
			5	LDO5OVC FALL MASK	
			6	V5EXT CONTROL RISE MASK	
			7	V5EXT CONTROL FALL MASK	

Run-Time-Address	Flash Address	Name	Bits	Description	Type
FFAA		INREG_INT[7:0]	0	IN REGULATION Channel 1	R/W
			1	IN REGULATION Channel 2	
			2	IN REGULATION Channel 3	
			3	IN REGULATION Channel 4	
			4	OUT OF REGULATION Channel 1	
			5	OUT OF REGULATION Channel 2	
			6	OUT OF REGULATION Channel 3	
			7	OUT OF REGULATION Channel 4	
FFAB	177	INREG_MASK[7:0]	0	IN REGULATION Channel 1 MASK	R/W
			1	IN REGULATION Channel 2 MASK	
			2	IN REGULATION Channel 3 MASK	
			3	IN REGULATION Channel 4 MASK	
			4	OUT OF REGULATION Channel 1 MASK	
			5	OUT OF REGULATION Channel 2 MASK	
			6	OUT OF REGULATION Channel 3 MASK	
			7	OUT OF REGULATION Channel 4 MASK	
FFAC		GEN_INT[4:0]	0	I2C INTERRUPT	R/W
			1	RESERVED	
			2	VCO PLL INTERRUPT	
			3	AUVLO RISE INTERRUPT	
			4	AUVLO FALL INTERRUPT	
FFAD	178	GEN_MASK[4:0]	0	I2C INTERRUPT MASK	R/W
			1	RESERVED	
			2	VCO PLL INTERRUPT MASK	
			3	AUVLO RISE INTERRUPT MASK	
			4	AUVLO FALL INTERRUPT MASK	
FFAE		RESERVED			
FFAF	179	TIMER_MASK[1:0]	0	TIMER1_MASK	R/W
			1	TIMER2_MASK	
FFB0		RESERVED			
FFB1		GPIO_PSIO_INT[7:0]	0	GPIO0 INTERRUPT	R/W
			1	GPIO1 INTERRUPT	
			2	PSIO0 INTERRUPT	
			3	PSIO1 INTERRUPT	
			4	PSIO2 INTERRUPT	
			5	RESERVED	
			6	RESERVED	
			7	RESERVED	
FFB2	17A	GPIO_PSIO_MASK[7:0]	0	GPIO0 INTERRUPT MASK	R/W
			1	GPIO1 INTERRUPT MASK	
			2	RESERVED	
			3	RESERVED	
			4	PSIO0 INTERRUPT MASK	
			5	PSIO1 INTERRUPT MASK	
			6	PSIO0 INTERRUPT MASK	
			7	RESERVED	

Run-Time-Address	Flash Address	Name	Bits	Description	Type
			1:0	RESERVED	
			2	CHIP_READY	
			3	FW_SOFT_RESET	
FFB4		I2C_RESETS[1:0]	0	I2C RESET	R/W
			1	RESERVED	
FFB5		I2CS_STS [7:0]	0	FIFO LEVEL INTERRUPT STATUS	R
			1	TRANSFER IN PROGRESS	
			2	RECEIVE FIFO EMPTY	
			3	TRANSMIT FIFO EMPTY	
			4	RECEIVE FIFO HALF FULL	
			5	TRANSMIT FIFO FULL	
			6	RECEIVE FIFO FULL	
			7	RECEIVE ACKNOWLEDGE	
FFB6		I2CS_DR[7:0]	7:0	I2C DATA	
FFB7		I2CS_ADDR[6:0]	6:0	I2C ADDRESS	
FFB8		RESERVED			
FFB9		I2CS_CTL[6:0]	0	I2C READ	R
			1	I2C WRITE	R
			5: 2	RESERVED	
			6	I2C INTERRUPT SOURCE	
FFBA		RESERVED			
FFBB		RESERVED			
FFBC		RESERVED			
FFBD		RESERVED			
FFBE		RESERVED			
FFBF		RESERVED			
FFC2		CH_DYN_UPDATE[3:0]	0	DYNAMIC UPDATE Channel 1	R/W
			1	DYNAMIC UPDATE Channel 2	
			2	DYNAMIC UPDATE Channel 3	
			3	DYNAMIC UPDATE Channel 4	
FFC3		FLASH CONTROL[7:0]	0	FLASH READ	R/W
			1	FLASH ERASE VERIFY	
			2	FLASH PROGRAM VERIFY	
			3	FLASH ERASE	
			4	FLASH ENABLE	
			5	RESERVED	
			6	RESERVED	
			7	FLASH PROGRAM SET	
FFC4		RESERVED			
FFC5		RESERVED			
FFC6		FLASH WRITE[1:0]	0	FLASH CLOCK ONLY ON WORD	R/W
			1	FLASH A WRITE ADDRESS ENABLE	
FFC7		RESERVED			
FFC8		RESERVED			
FFC9		RESERVED			
FFCA		RESERVED			
FFCB		RESERVED			
FFCC		RESERVED			

Run-Time-Address	Flash Address	Name	Bits	Description	Type
FFCD		RESERVED			
FFCE		FAULT_FLAG_CLEAR[7:0]	0	OVP FAULT CLEAR Channel 1	R/W
			1	OVP FAULT CLEAR Channel 2	
			2	OVP FAULT CLEAR Channel 3	
			3	OVP FAULT CLEAR Channel 4	
			4	UVLO WARNING CLEAR	
			5	UVLO FAULT CLEAR	
			6	OTP WARNING CLEAR	
			7	OTP FAULT CLEAR	
FFCF		GPIO_VALUE_IN[5:0]	0	GPIO VALUE IN	R
			1	GPI1 VALUE IN	
			2	PSIO0 VALUE IN	
			3	PSIO1 VALUE IN	
			4	PSIO2 VALUE IN	
			5	RESERVED	
FFD0		RESERVED			
FFD1		RESERVED			
FFD2		ON_DEMAND_SAMPLE[4:0]	0	ON DEMAND SAMPLE VIN	R/W
			1	ON DEMAND SAMPLE TEMP	
			2	ON DEMAND SAMPLE VOUT	
			4:3	AUX VOUT CHANNEL SELECT[1:0] 00 Channel 1 01 Channel 2 10 Channel 3 11 Channel 4	
FFD3		OCP_CLEAR[7:0]	0	OCP WARNING Channel 1 CLEAR	R/W
			1	OCP WARNING Channel 2 CLEAR	
			2	OCP WARNING Channel 3 CLEAR	
			3	OCP WARNING Channel 4 CLEAR	
			4	OCP FAULT Channel 1 CLEAR	
			5	OCP FAULT Channel 2 CLEAR	
			6	OCP FAULT Channel 3 CLEAR	
			7	OCP FAULT Channel 4 CLEAR	
FFD4		CLOCK_CONTROL[2:0]	0	RESERVED	
			1	VCO PLL CYCLE LIMIT	R/W
			2	VCO PLL LOCKING SUCCESS	R
FFD5		GPIO_VALUE_OUT[5:0]	0	Bit 0 – GPIO0 VALUE OUT	R/W
			1	GPIO1 VALUE OUT	
			2	PSIO0 VALUE OUT	
			3	PSIO1 VALUE OUT	
			4	PSIO2 VALUE OUT	
			5	RESERVED	
FFD6		RESERVED			
FFD7		I2CS_PEC_ACK[7:0]	0	PEC ACKNOWLEDGE	R/W
			1	SLAVE MATCH REGISTER	R
			7:2	RESERVED	
FFD8		RESERVED			
FFD9		RESERVED			

Run-Time-Address	Flash Address	Name	Bits	Description	Type
FFDA		CH_ENABLE[3:0]	0	ENABLE Channel 1	R/W
			1	ENABLE Channel 2	
			2	ENABLE Channel 3	
			3	ENABLE Channel 4	
FFDB		FW_SLAM_DWN[7:0]	0	FIRMWARE SLAM DOWN Channel 1	R/W
			1	FIRMWARE SLAM DOWN Channel 2	
			2	FIRMWARE SLAM DOWN Channel 3	
			3	FIRMWARE SLAM DOWN Channel 4	
			4	ADC CLOCK GATE ENABLE	
			5	FIRMWARE POWER DOWN AT AUVLO	
			6	MUX HARDWARE POWER DOWN AT AUVLO Selects between two hardware power down options. 0 Channel enabled 1 PWM channel enabled	
			7	MUX POWER DOWN AT AUVLO Selects between two power down options. 0 Hardware power down 1 Firmware power down	
FFDC	17B	FAULT_IGNORE[3:0]	0	OVP IGNORE	R/W
			1	OCP IGNORE	
			2	OTP IGNORE	
			3	UVLO IGNORE	

2.32 Monitoring Registers

These registers can be used to read the XRP7724 status and hardware monitoring values.

Runtime Address	Name	Bits	Description
D501	READ_IL_CH0[6:0]	6:0	Channel 1 Inductor Current Reading. 1.25mV/2.5mV per bit depending on range
D502	READ_IL_CH1[6:0]	6:0	Channel 2 Inductor Current Reading. 1.25mV/2.5mV per bit depending on range
D503	READ_IL_CH2[6:0]	6:0	Channel 3 Inductor Current Reading. 1.25mV/2.5mV per bit depending on range
D504	READ_IL_CH3[6:0]	6:0	Channel 4 Inductor Current Reading. 1.25mV/2.5mV per bit depending on range
D505	READ_VOUT_CH0[6:0]	6:0	Channel 1 Output Voltage Reading. 15mV/30mV/60mV per bit depending on range
D506	READ_VOUT_CH1[6:0]	6:0	Channel 2 Output Voltage Reading. 15mV/30mV/60mV per bit depending on range
D507	READ_VOUT_CH2[6:0]	6:0	Channel 3 Output Voltage Reading. 15mV/30mV/60mV per bit depending on range
D508	READ_VOUT_CH3[6:0]	6:0	Channel 4 Output Voltage Reading. 15mV/30mV/60mV per bit depending on range
D509	READ_VIN[6:0]	6:0	Input Voltage Reading. 200mV per bit

Runtime Address	Name	Bits	Description
D50A	READ_VTJ[6:0]	6:0	Temperature Reading. 5K per bit
D50B	READ_PFM_PERIOD_CH0[7:0]	7:0	Channel 1 PFM Period Length. 25MHz/8 switching cycles or units of 320ns
D50C	READ_PFM_PERIOD_CH1[7:0]	7:0	Channel 2 PFM Period Length. 25MHz/8 switching cycles or units of 320ns
D50D	READ_PFM_PERIOD_CH2[6:0]	6:0	Channel 3 PFM Period Length. 25MHz/8 switching cycles or units of 320ns
D50E	READ_PFM_PERIOD_CH3[7:0]	7:0	Channel 4 PFM Period Length. 25MHz/8 switching cycles or units of 320ns
D50F	READ_VFDBK_ADC[7:0]	7:0	Latched ADC Feedback. data = xr24.read_reg(0xD50F) data_lsb = data & 15 data_msb = (data & 240)>>1 final_data = data_lsb + data_msb
D510	READ_AUX_ADC[6:0]	6:0	Latched aux ADC. data = xr24.read_reg(0xD510) data_lsb = data & 15 data_msb = (data & 240)>>1 final_data = data_lsb + data_msb
D511	V5EXT_CTRL	0	V5EXT status
D512	READ_POWER_GOOD[3:0]	0	Channel 1 power good status
		1	Channel 2 power good status
		2	Channel 3 power good status
		3	Channel 4 power good status
D513	READ_CONTROL_MODE_CH0[3:0]	0	Channel 1 steady state PWM
		1	Channel 1 PFM
		2	Channel 1 Under Voltage OVS mode
		3	Channel 1 Over Voltage OVS mode
D514	READ_CONTROL_MODE_CH1[3:0]	0	Channel 2 steady state PWM
		1	Channel 2 PFM
		2	Channel 2 Under Voltage OVS mode
		3	Channel 2 Over Voltage OVS mode
D515	READ_CONTROL_MODE_CH2[3:0]	0	Channel 3 steady state PWM
		1	Channel 3 PFM
		2	Channel 3 Under Voltage OVS mode
		3	Channel 3 Over Voltage OVS mode
D516	READ_CONTROL_MODE_CH3[3:0]	0	Channel 4 steady state PWM
		1	Channel 4 PFM
		2	Channel 4 Under Voltage OVS mode
		3	Channel 4 Over Voltage OVS mode
D517	READ_ULTRASONIC_MODE[3:0]	0	Channel 1 Ultrasonic mode
		1	Channel 2 Ultrasonic mode
		2	Channel 3 Ultrasonic mode
		3	Channel 4 Ultrasonic mode

Document Revision History

Revision	Date	Description
1.0.0	3/27/15	Initial release

www.exar.com

48760 Kato Road
Fremont, CA 94538
USA

Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7001
Email: Support@exar.com